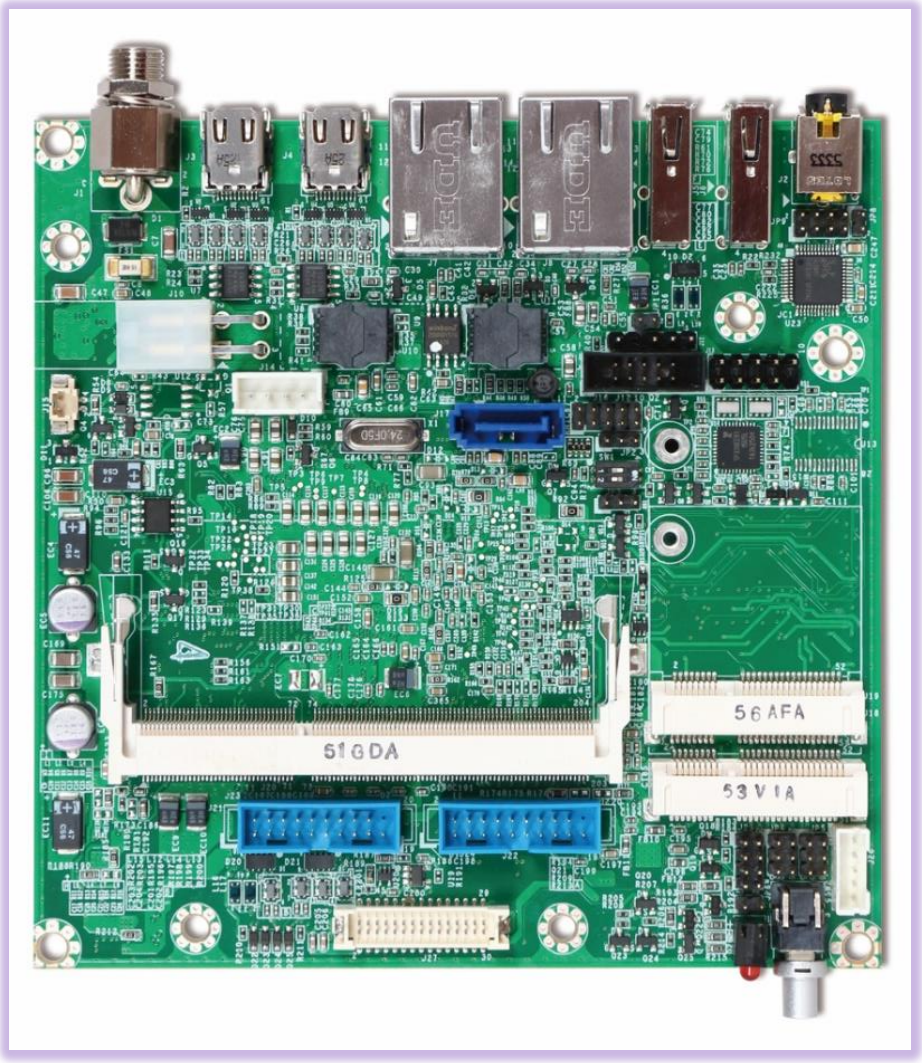

NANO-6050

Portwell

Version 1.2

Revision History

R0.1	Preliminary
R1.0	Add USB 3.0 pin define, add EMI/ESD certification
R1.1	Revised mSATA and mini-PCIe location on page 16
R1.2	Revised typo

Contents

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the NANO-6050. This document should be referred to when designing NANO-ITX application. The other reference documents that shouldbe used include the following:

- ✧ Intel Broadwell-U Guide
- ✧ Intel Broadwell-U Specification

Please contact Portwell Sales Representative for above documents.

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1 Introduction

Portwell Inc., a world-leading innovator in the Industrial PC (IPC) market and a member of the Intel® Communications Alliance, has launched its new NANO-ITX form factor, 120mmX120mm size, based NANO-6050 for embedded system board (ESB) that offers lower power consumption, robust computing power and with longevity support.

The NANO-6050 is specifically designed to operate at low power consumption and low heat, so it can be a truly fanless configuration and battery operated. NANO-6050 is designed with Intel(R) 5th Generation Intel® Core™ i3-5010U and Intel® Core™i5-5350U, Processor code named Broadwell U-series. Based on 5th Generation Intel® Core™ SoC, the NANO-6050 supports one DDR3L SODIMM socket up to 8GB system memory and comes with one SATA III, one mSATA socket, one half size mini-PCIe, triple display by two mini-DP and one LVDS, two gigabit Ethernet, and six USB ports (two for 2.0 on rear I/O, four for 3.0 on board). It also built with DC 12V or ATX 12V input.

Base on leading Intel® Core™ SoC, NANO-6050 is a compact and low power dissipation board for Digital Signage, Digital Security Surveillance (DSS) and Medical applications…etc.

2 Specifications

Main Processor	◆ Intel® 5th Generation Intel® Core™ i5/i3 Processors
System BIOS	◆ AMI BIOS
Main Memory	◆ Up to 8 GB in oneSODIMM sockets. ◆ Supports DDR3L 1333/1600 MHz.
Graphics	◆ Next Generation Intel® HD Graphics with OpenCL 2.0, OpenGL 4.0 and DirectX11.1 support; up to three independent displays. High performance hardware MPEG-2 decoding, WMV9 (VC-1) and H.264 (AVC) support Blue-ray support @ 40 MBit/s ◆ Intel® HD Graphics 6000/5500 Processor (300MHz) ◆ Mini-DP up to 3840x2160 ◆ LVDS (eDP to LVDS) up to 2 x 24bit
Expansion Interface	◆ One half size Mini-PCIe
SATA Interface	◆ One SATA ports(SATA 6Gb/s) ◆ One mSATA (SATA 6Gb)
Input/output	◆ Serial Ports: One serial ports, RS-232/422/485, switched by BIOS ◆ USB Port: 2 x USB 2.0 on rear I/O, 4 x USB 3.0 on board ◆ Audio Interface: Audio Combo Jack including Mic-in and Line-out. Connector for Mic-In, Line-In and Line-Out.

Ethernet	◆ Supports dual 10/100/1000 Mbps Ethernet ports via PCI Express x1 bus. ◆ Controller:LAN1: Intel I218; LAN2: Intel I218
High Drive GPIO	◆ One pin-header for 8 bit GPIO(4bit in & 4bit out)
Mechanical and environmental specifications	◆ Operating temperature: 0 ~ 60° C ◆ Storage temperature:-20 ~ 80° C ◆ Humidity: 5 ~ 90% non-condensing ◆ Power supply voltage: +12 V ◆ Board size: 120mm x 120 mm (4.72" x 4.72")
EMI/ESD	◆ ESD: IEC 61000-4-2:2008 ◆ EMI: EN 55022: 2010/ AC:2011 Class B

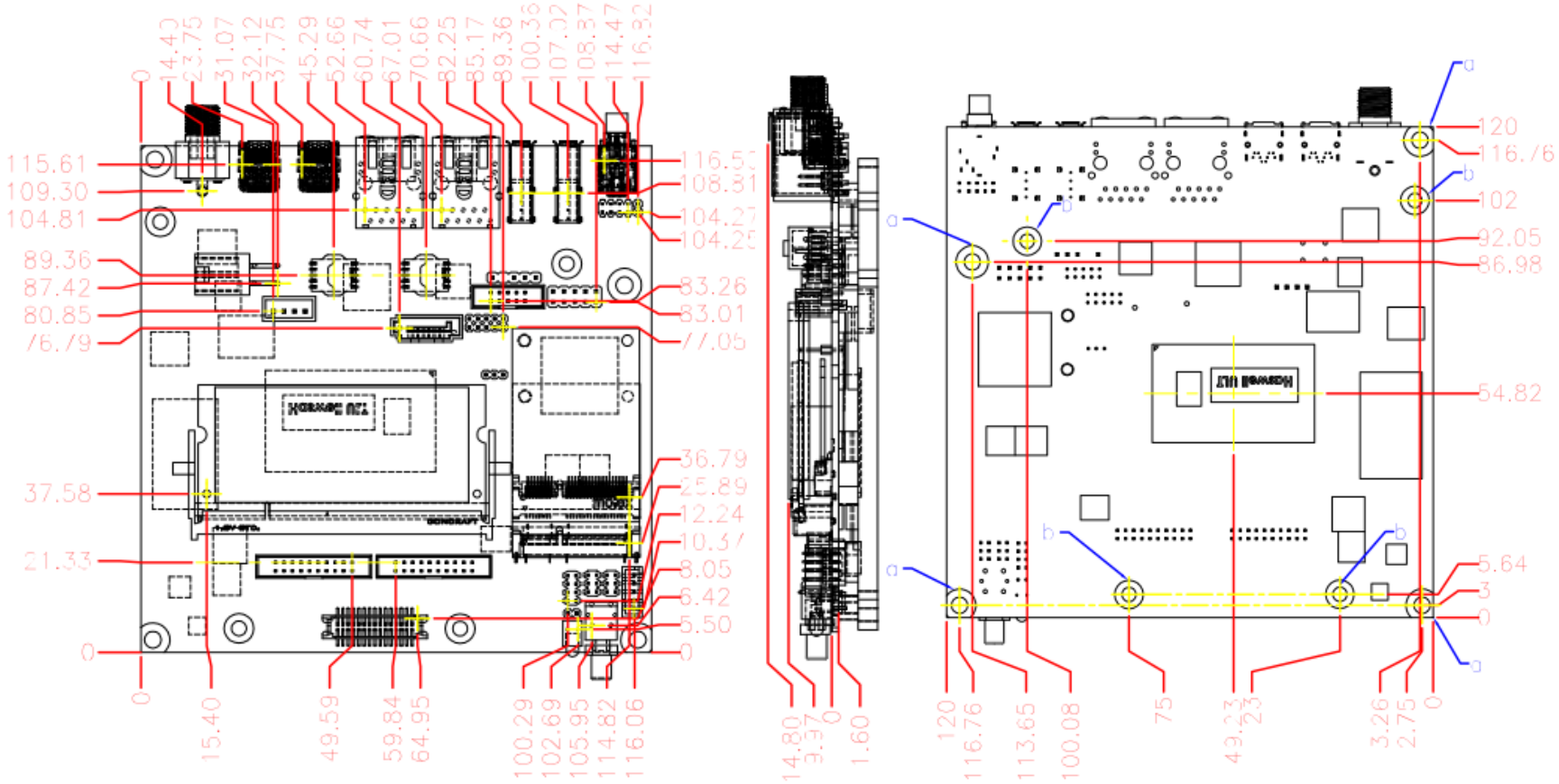
2.1 Supported Operating Systems

The NANO-6050 supports the following operating systems.

- Windows* 8.1u (64 bit)
- * Windows* Embedded Industry 8.1 (64 bit)
- Windows* 7 (32/64 bit)
- Windows* 7 (POS ready 7 & WES7) (32/64 bit)
- Windows 10* (64 bit)
- Fedora* (19 or later) Distribution (64 bit)
- Ubuntu*, SuSe Enterprise*, Red hat* Enterprise (64 bit)
- ** Yocto* Tool-based Embedded Linux Distribution (64 bit)
- VxWorks* (RTOS) (64 bit)

* Microsoft* Windows* 7 does not natively support the LPSS bus on 5th Gen Intel® Core™ Processors (U-Series).
** Commercial Linux* Support provided by Wind River* Systems.

2.2 Mechanical Dimensions



2.3 Power consumption

Test Configuration	
CPU Type	Intel® Core™ Broadwell i7-5650U CPU @ 2.20GHz 256KB 100MHz
SBC BIOS	Portwell, Inc. NANO-6050 TEST BIOS (50604T01)
Memory	WARIS DDR3L SO-DIMM 1600 1.35V/8GB*1 (SK hynix H5TC4G83AFR)
VGA Card	Onboard Intel® Graphics 6000
VGA Driver	Intel® Graphics 6000 ,Ver:10.18.14.4156
LAN Card	Onboard Intel® Ethernet Connection I218-LM
LAN Driver	Intel® Ethernet Connection I218-LM ,Ver:12.12.80.19
LAN Card	Onboard Intel® I210 Gigabit Network connection
LAN Driver	Intel® I210 Gigabit Network connection, Ver:12.11.97.1
Audio Card	Onboard Realtek High Definition Audio
Audio Driver	Realtek High Definition Audio Device, Ver:6.0.1.7512
Chip Driver	Intel® Chipset Device Software Ver:10.0
USB3.0 Driver	Intel® USB3.0 extensible Host Controller Ver:3.0.5.69
EC Version	IT8528 50527T00
USB-DVDROM	Pioneer DVR-XT11T
Power Supply	FSP Power Adapter FSP120-AHAN1

Power consumption			
Item	**Power ON**	**Full Loading 10Min**	**Full Loading 30Min**
ATX Power	1.54A	2.06A	2.15A

2.4Environmental Specifications

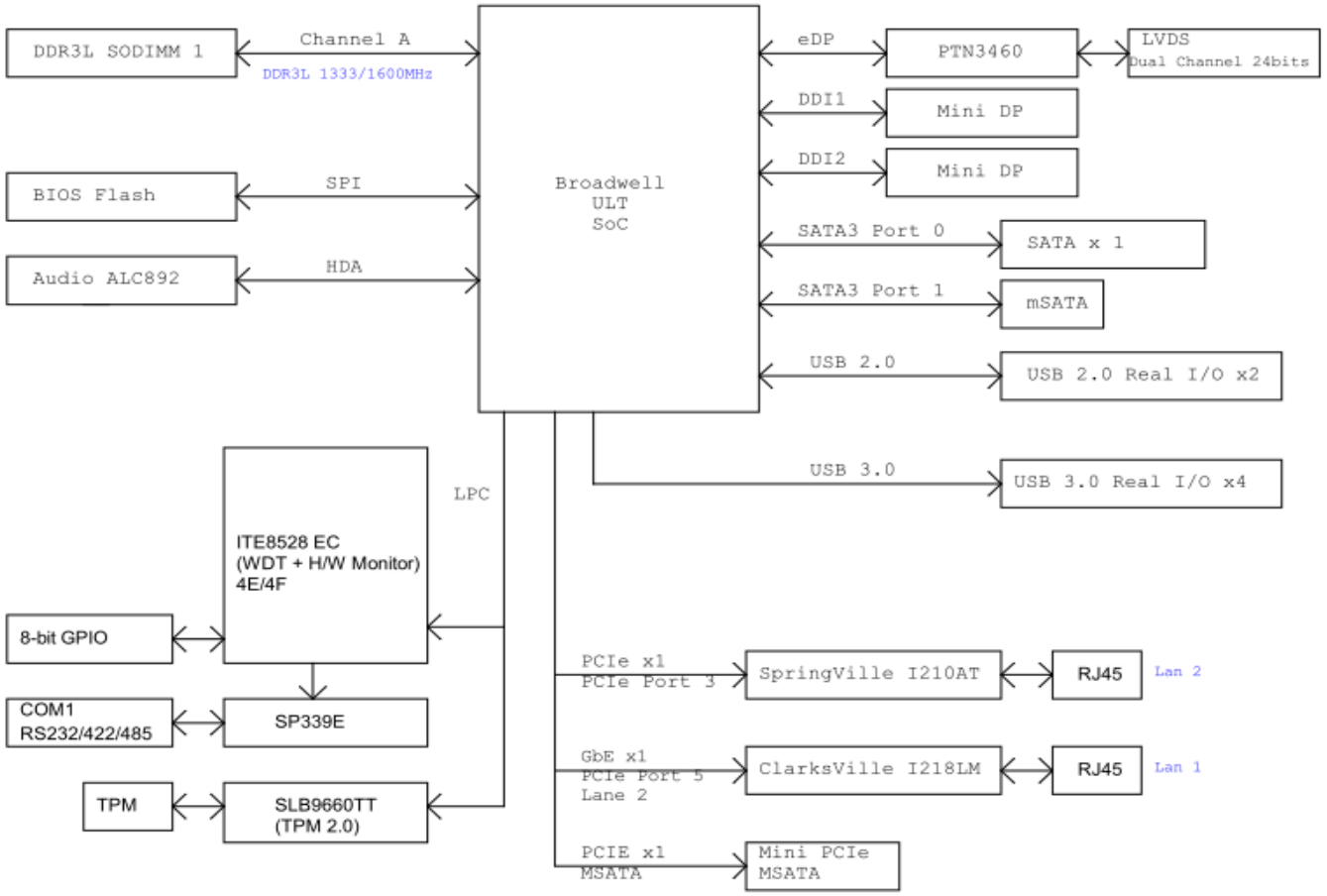
Storage Temperature: -20~80°C

Operation Temperature: 0~60°C

Storage Humidity: 5~90%

Operation Humidity: 10~90%

3 Block Diagram



4Hardware Configuration

4.1 Jumpers and Connectors

This chapter indicates jumpers' headers' and 'connectors' locations. Users may find useful information related to hardware settings in this chapter.

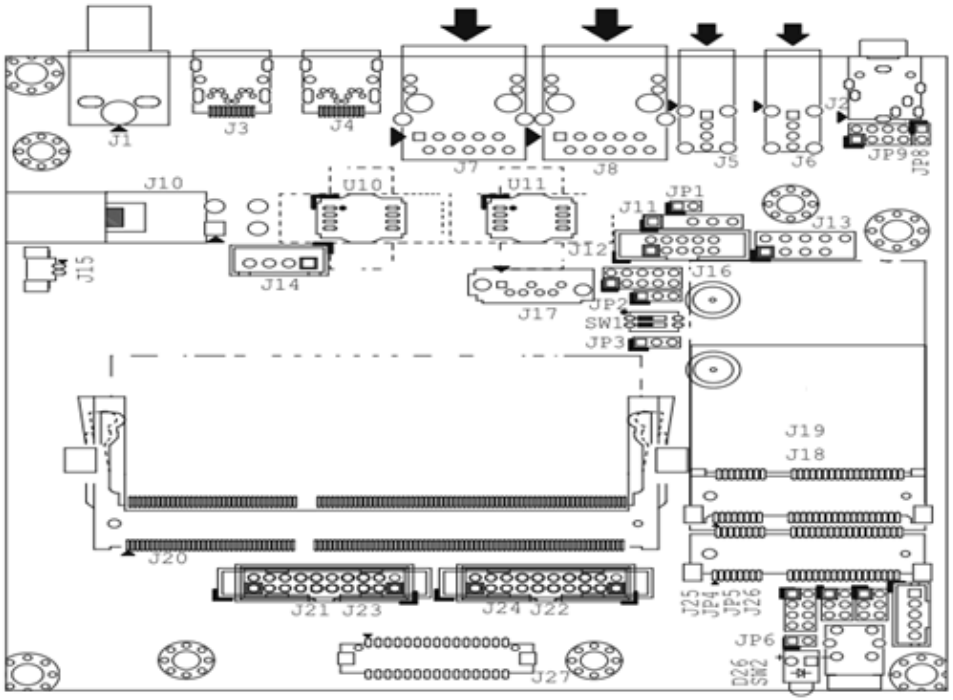


Figure 1, NANO-6050 Top View

4.2Jumper Settings

For users to customize NANO-6050's features. In the following sections, **Short** means covering a jumper cap over jumper pins; **Open** or **N/C** (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 1 for the Jumper allocations.

Jumper Table

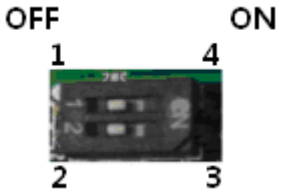
The jumper settings are schematically depicted in this manual as follows:

Jump Function List:

Jump	Function	Remark
J1	DC Jack	+12V Input
J2	Audio Jack (Lineout + Mic)	Follow CTIA Specification Please do not use JP9 and J2 at the same time
J3	Mini DP Connector#1	
J4	Mini DP Connector#2	
J5	USB 2.0 Connector	
J6	USB 2.0 Connector	
J7	RJ45#1 (I210-LAN) Connector	
J8	RJ45#2 (I218-LAN) Connector	
J10	ATX 4 Pin Connector	+12V Input
J11	SMBus Pin HDR.	1x5 pin header (Pitch = 2.0mm)
J12	RS232/422/485 Pin HDR.	5x2 pin header (Pitch = 2.0mm)

J13	LPC Pin HDR.	5x2 pin header (Pitch = 2.54mm)
J14	SATA Power Connector	1x4 pin header (Pitch = 2.54mm)
J15	Battery Connector	
J16	GPIO Pin HDR.	5x2 pin header (Pitch = 2.0mm)
J17	SATA Connector	Support SATA 3.0
J18	mSATA Connector	Support SATA 3.0
J19	Mini PCIe Connector	Support PCIe 2.0 and USB 2.0
J20	DDR3L SO-DIMM Socket(Non-ECC)	Support DDR3L-1333/1600
J21/J23	External USB 3.0 Pin HDR.	
J22/J24	External USB 3.0 Pin HDR.	
J25	Front Panel Pin HDR	4x2 pin header (Pitch = 2.0mm)
J26	LVDS Backlight Power Pin HDR.	
J27	LVDS Connector	
JP1	Watch Dog Timer Enable	
JP2	General Purpose Output Voltage Selection	
JP3	CMOS CLEAR	
JP4	Panel Backlight Enable Selection	
JP5	Panel Voltage Selection	
JP6	S0 State Led	
JP8	Mic in LEFT Channel and Mic in Right Jumper	See JP8
JP9	External Audio (Mic + Line_in + Line_out) Pin HDR.	Please do not use JP9 and J2 at the same time
SW1	AT Mode or ATX Mode Selection	
SW2	Power Button	

SW1: AT Mode or ATX Mode Selection



PIN No.	Signal Description
1-4 ON 2-3 ON	ATX Mode
1-4 ON 2-3 OFF	ATX Mode
1-4 OFF 2-3 ON	ATX Mode
1-4 OFF **2-3 OFF**	**AT Mode**

JP1: Watch Dog Timer Hardware Enable

PIN No.	Signal Description
1-2 short	**Enable**
1-2 open	Disbale

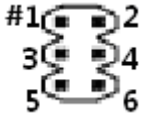
JP2: General Purpose Output (GPO) Voltage Selection

PIN No.	Signal Description
1-2 short	5V
2-3 short	**3.3V**

JP3: CMOS Clear

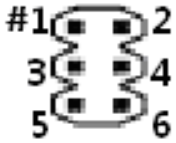
PIN No.	Signal Description
1-2 short	**Normal Operation**
2-3 short	Clear CMOS Content

JP4: Panel Backlight Enable Selection



PIN No.	Signal Description
1-3 , 2-4	**5V , Active High**
3-5 , 2-4	5V , Active Low
1-3 , 4-6	12V , Active High
3-5 , 4-6	12V , Active Low

JP5: Panel Voltage Selection



PIN No.	Signal Description
1-3 short	3.3V
3-5 short	**5V**
3-4 short	12V

JP6: S0 State LED

PIN No.	Signal Description
1	3.3V
2	Gnd

JP8: Mic in LEFT Channel and Mic in Right Jumper

PIN No.	Signal Description
1	MIC_R
2	MIC_L

JP9: External Audio (Mic + Line in +Line out) Pin HDR.

PIN No.	Signal Description
1	MIC_L
2	LINE_IN_L
3	GND
4	LINE_IN_R
5	LINE_OUT_L
6	GND
7	LINE_OUT_R
8	MIC_R

Recommend:

(a) When using J2 for Mic out function, please use jumper shunt to short JP8 Pin 1 and Pin 2.

(b) When Using JP9 for Mic out function, please do not short JP8.

(c)Please do not use JP9 and J2 at the same time.

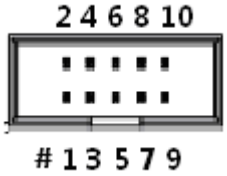
J10: ATX 4 Pin Power Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GND	2	GND
3	+12V	4	+12V

J11: SMBus Pin HDR

PIN No.	Signal Description
1	SMB_CLK
2	NC
3	GND
4	SMB_DATA
5	3.3V

J12: RS232/422/485 Pin HDR.

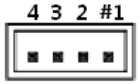


PIN No.	Signal Description
1	DCD#1/DT-
2	RXD#1/DT+
3	TXD#1/422R+
4	DTR#1/422R-
5	GND
6	DSR#1
7	RTS#1
8	CTS#1
9	RI#
10	NC

J13: LPC Pin HDR.

PIN No.	Signal Description
1	LAD0
2	3V
3	LAD1
4	PLTRST#
5	LAD2
6	LFRAME#
7	LAD3
8	LPCCLK
9	NC
10	GND

J14: SATA Power Connector

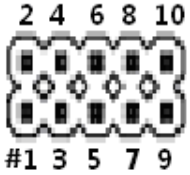


PIN No.	Signal Description
1	12V
2	GND
3	GND
4	5V

J15: Battery Connector

PIN No.	Signal Description
1	3V
2	GND

J16: GPIO Pin HDR.

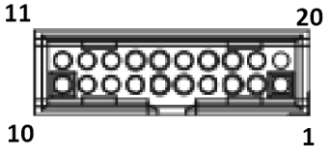


PIN No.	Signal Description
1	GPI#0
2	GPO#0
3	GPI#1
4	GPO#1
5	GPI#2
6	GPO#2
7	GPI#3
8	GPO#3
9	GND
10	5V

Note:

GPO Operating Voltage can be switched by JP2

J22 J23 J24 J25: External USB 3.0 Pin HDR

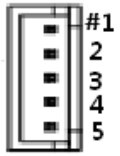


PIN No.	Signal Description	PIN No.	Signal Description
1	5V	11	USB2_DP#2
2	USB3_RX_DN#1	12	USB2_DN#2
3	USB3_RX_DP#1	13	Ground
4	Ground	14	USB3_TX_DP#2
5	USB3_TX_DN#1	15	USB3_TX_DN#2
6	USB3_TX_DP#1	16	Ground
7	Ground	17	USB3_RX_DP#2
8	USB2_DN#1	18	USB3_RX_DN#2
9	USB2_DP#1	19	5V
10	Ground	20	Key

J25: Front Panel Pin HDR

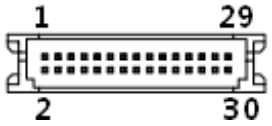
PIN No.	Signal Description
1	VCC5
2	SATA_LED#
3	5V
4	Buzzer
5	Reset#
6	GND
7	GND
8	Power On#

J26: LVDS Backlight Power Pin HDR.



PIN No.	Signal Description
1	5V
2	Backlight Control
3	12V
4	GND
5	Backlight Enable

J27: LVDS Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	VDD_LVDS	2	VDD_LVDS
3	LVDSA_DATA0	4	LVDSA_DATA#0
5	LVDSA_DATA1	6	LVDSA_DATA#1
7	LVDSA_DATA2	8	LVDSA_DATA#2
9	LVDSA_DATA3	10	LVDSA_DATA#3
11	LVDSA_CLKP	12	LVDSA_CLKN
13	DDC_SCL	14	DDC_SDA
15	GND	16	GND
17	LVDSB_DATA0	18	LVDSB_DATA#0
19	LVDSB_DATA1	20	LVDSB_DATA#1
21	LVDSB_DATA2	22	LVDSB_DATA#2
23	LVDSB_DATA3	24	LVDSB_DATA#3
25	LVDSB_CLKP	26	LVDSB_CLKN
27	N/C	28	N/C
29	GND	30	GND

5 SignalDescriptions

5.1 Watch Dog Signal

WDT Control Command Example

```
#include <stdio.h>
#include <stdlib.h>
#include <conio.h>
#include <dos.h>

#define EC_DATA          0x62
#define EC_CMD           0x66
#define EC_CMD_READ   0x80
#define EC_CMD_WRITE       0x81

#define  WDT_MODE             0x06    // WDT Select mode.
#define  WDT_MIN              0x07    // Minute mode counter
#define  WDT_SEC          0x08    // Second mode counter

// Use port 62 and port 66 to access EC command / data.
static intIBF_Check()
{
```

```
    unsigned char IBF_status;
    do
    {
        pw_udelay (20);    // delay 20 us
        outportb (EC_CMD, &IBF_status);
    } while (IBF_status& 0x02);
    return 1;
}

static intOBF_Check ()
{
    unsigned char OBF_status;
    do
    {
        pw_udelay (20);    // delay 20 us
        OBP_status = inportb (EC_CMD);
    } while (!(OBF_status& 0x01));
    return 1;
}

static void Write_EC (unsigned char index, unsigned char data)
{
    IBF_Check ();
```

```
    outportb (EC_CMD, EC_CMD_WRITE);
    IBF_Check ();
    outportb (EC_DATA, index);
    IBF_Check ();
    outportb (EC_DATA, data);
}

static unsigned char Read_EC (unsigned char address)
{
    unsigned char data;
    IBF_Check ();
    outportb (EC_CMD, EC_CMD_READ);
    IBF_Check ();
    outportb (EC_DATA, address);
    OBF_Check();
    data = inportb (EC_DATA);
    return data;
}

void EC_WDT_Trigger ()
{
    /* WDT Counter */
    Write_EC (WDT_SEC, 0x05);
```

```
    /* if use minute mode */
    /* Write_EC (WDT_MIN, 0x05); */

    /* 0x01 is second mode */
    /* 0x03 is minute mode */
    Write_EC (WDT_MODE, 0x01);
}

Write_EC ((b->wdt.ec.count_m_addr& 0xFF), b->wdt.ec.timeout);
            Write_EC ((b->wdt.ec.cfg_addr& 0xFF), 0x03); // WDTCFG[1:0]=11
int main ()
{
inti;
    EC_WDT_Trigger ();
    for (i = 0; i< 5; i++)
    {
        printf ("Reset counter .....%d\n", 5 - i);
        delay (1000);
    }
    return 0;
}
```

5.2 GPIO Signal

GPIO Control Command Example (C Language)

```
#include <stdio.h>
#include <stdlib.h>
#include <conio.h>
#include <dos.h>

#define EC_DATA              0x62
#define EC_CMD               0x66
#define EC_CMD_READ          0x80
#define EC_CMD_WRITE         0x81

#define GPIO_DIR             0x2B
#define GPIO_DATA            0x2C

static void Write_EC (unsigned char index, unsigned char data)
{
```

```
        delay(100);
outportb (EC_CMD, EC_CMD_WRITE);
        delay(100);
outportb (EC_DATA, index);
        delay(100);
outportb (EC_DATA, data);
}

static unsigned char Read_EC (unsigned char address)
{
        unsigned char data;
        delay(100);
outportb (EC_CMD, EC_CMD_READ);
        delay(100);
outportb (EC_DATA, address);
        delay(100);
        data = inportb (EC_DATA);
```

```
	return data;
}

int main ()
{
	unsigned char d2;
printf("\n\n");
printf("NANO-6050 GPIO TEST Program v1.0\n");
printf("Please short the following pins with 2.0mm-pitched jumper on J10\n");
printf("PIN 1,3,5,7 is input ; PIN 2,4,6,8 is output\n");
printf("GPIO1 ---- GPIO5\n");
printf("GPIO2 ---- GPIO6\n");
printf("GPIO3 ---- GPIO7\n");
printf("GPIO4 ---- GPIO8\n");
printf("GND      xxxxVcc<==PWR/GND pins, DO NOT short them!\n\n");
printf("Test Begins...\n");
```

```
	/* Set GPIO Port In/Out mode */
/* Port 1 ~ 4 In mode, 5 ~ 8 Out mode*/
Write_EC (GPIO_DIR, 0x0F);

	/* Set Port 5 ~ 8 Low */
Write_EC (GPIO_DATA, 0x0F);
	sleep(1);

	d2 = Read_EC (GPIO_DATA);

printf("GPIO_DATA = %x\n", d2);
	if ((d2 & 0x01) == 0)
printf ("GPIO70->GPIO74 test ok !! (pull low)\n");
	else
printf ("GPIO70->GPIO74 test fail (pull high) \n");

	if ((d2 & 0x02) == 0)
```

```
printf ("GPIO71->GPIO75 test ok !! (pull low)\n");
        else
printf ("GPIO71->GPIO75 test fail (pull high)\n");

        if ((d2 & 0x04) == 0)
printf ("GPIO72->GPIO76 test ok !! (pull low)\n");
        else
printf ("GPIO72->GPIO76 test fail (pull high)\n");

        if ((d2 & 0x08) == 0)
printf ("GPIO73->GPIO77 test ok !! (pull low)\n");
        else
printf ("GPIO73->GPIO77 test fail (pull high)\n");
        return 0;
}
```

6 System Resources

6.1 Intel® Broadwell-U CPU

Intel® Core™ i5-5350U Processor (2 core, 15W, 1.8GHz, 1600MT)
Intel® Core™ i3-5010U Processor (2 core, 15W, 2.1GHz, 1600MT)

6.2 Main Memory

NANO-6050 provides 1 x 204-pin SO-DIMM sockets which supports DDR3L non-ECC memory. The maximum memory can be up to 8GB. Memory clock and related settings can be detected by BIOS via SPD interface.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

6.3 Installing the Single Board Computer

To install your NANO-6050 into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position

Step 2 : Install and configure CPU and memory module on right position

Step 3 : Place NANO-6050 into the dedicated position in the system

Step 4 : Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that mother board is properly inserted and fixed by mechanism.

Note:

Please refer to section 6.3.1 to 6.3.4 to install INF/Graphic/LAN

6.3.1 Chipset Component Driver

NANO-6050 uses state-of-art Intel® Broadwell-U Soc. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows 8, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in NANO-6050 CD-title

6.3.2 Intel® HD Graphics 6000/5500

NANO-6050 has integrated Intel® HD Graphics 6000/5500 which supports DX11.2, OpenGL 4.3 / OpenCL 2.0. It is the most advanced design to gain an outstanding graphic performance. NANO-6050 supports VGA, Mini DP. This combination makes NANO-6050 an excellent performance hardware.

Drivers Support

Please find the Graphic driver in the NANO-6050 CD-title. The driver supports Windows 8.

6.3.3 Intel LAN I210IT/I218LM Gigabit Ethernet Controller

- Intel I210IT Gigabit Ethernet controller and 1x RJ45 connectors on rear I/O
- Intel I218LM Gigabit Ethernet controller and 1x RJ45 connectors on rear I/O

Drivers Support

Please find Intel I210IT/I218LM LAN driver in /Ethernet directory of NANO-6050 CD-title. The driver supports Windows 8.

7 BIOS Setup Items

7.1 Introduction

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

7.2 BIOS Setup

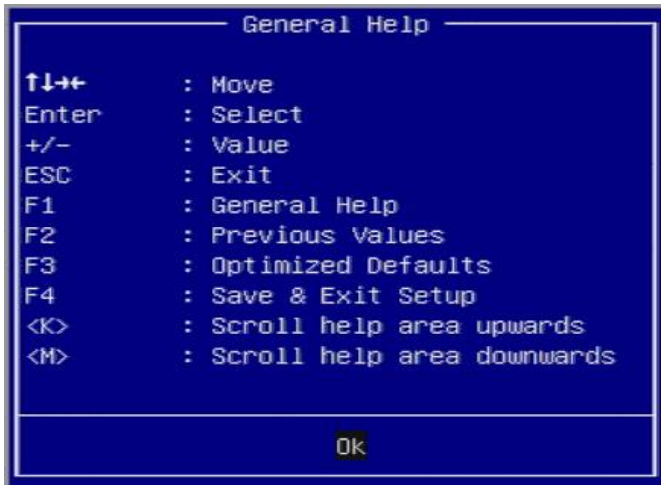
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <ESC> or <DELETE> key will enter BIOS setup screen.

Press <ESC> or <DELETE> to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

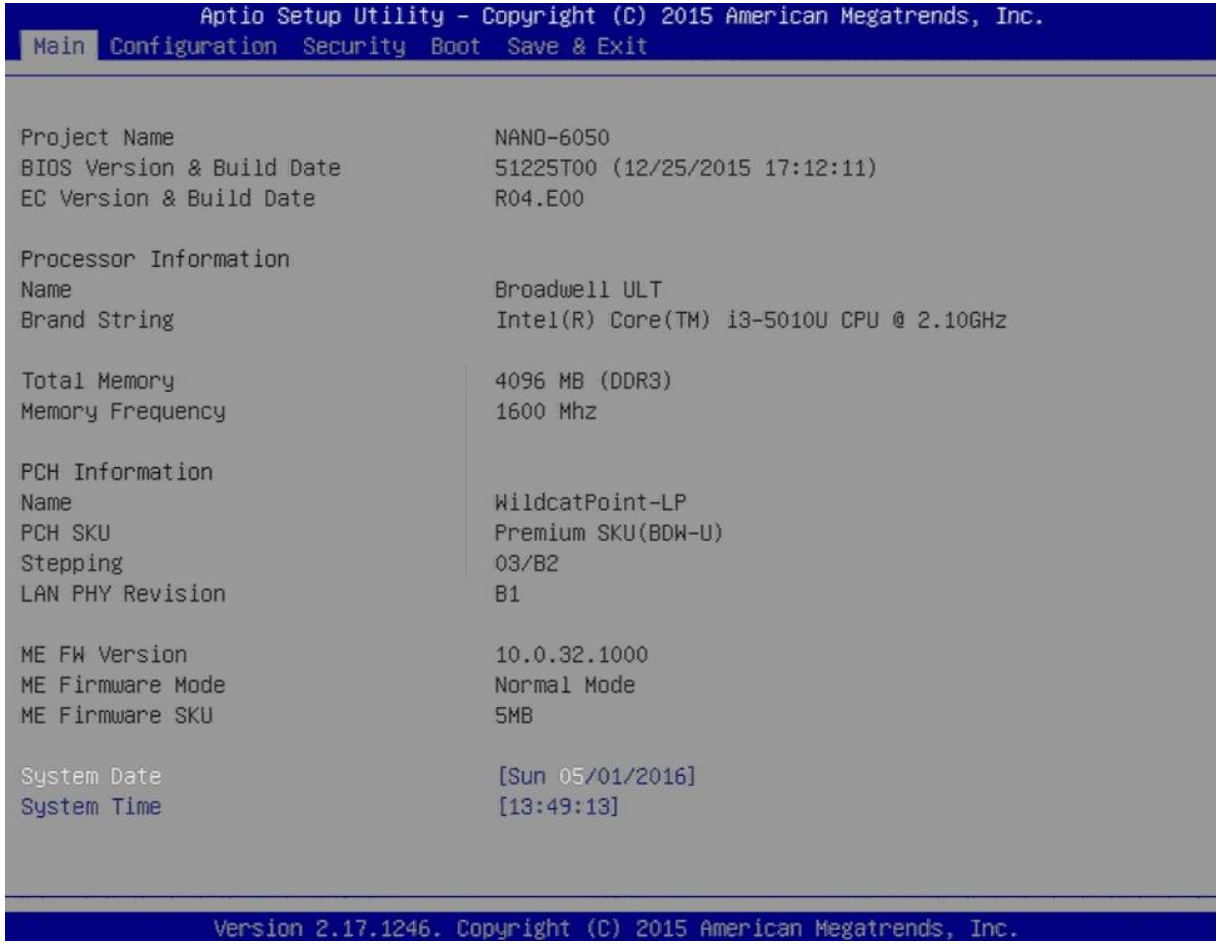
Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menuby pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help Screen.



7.2.1 Main

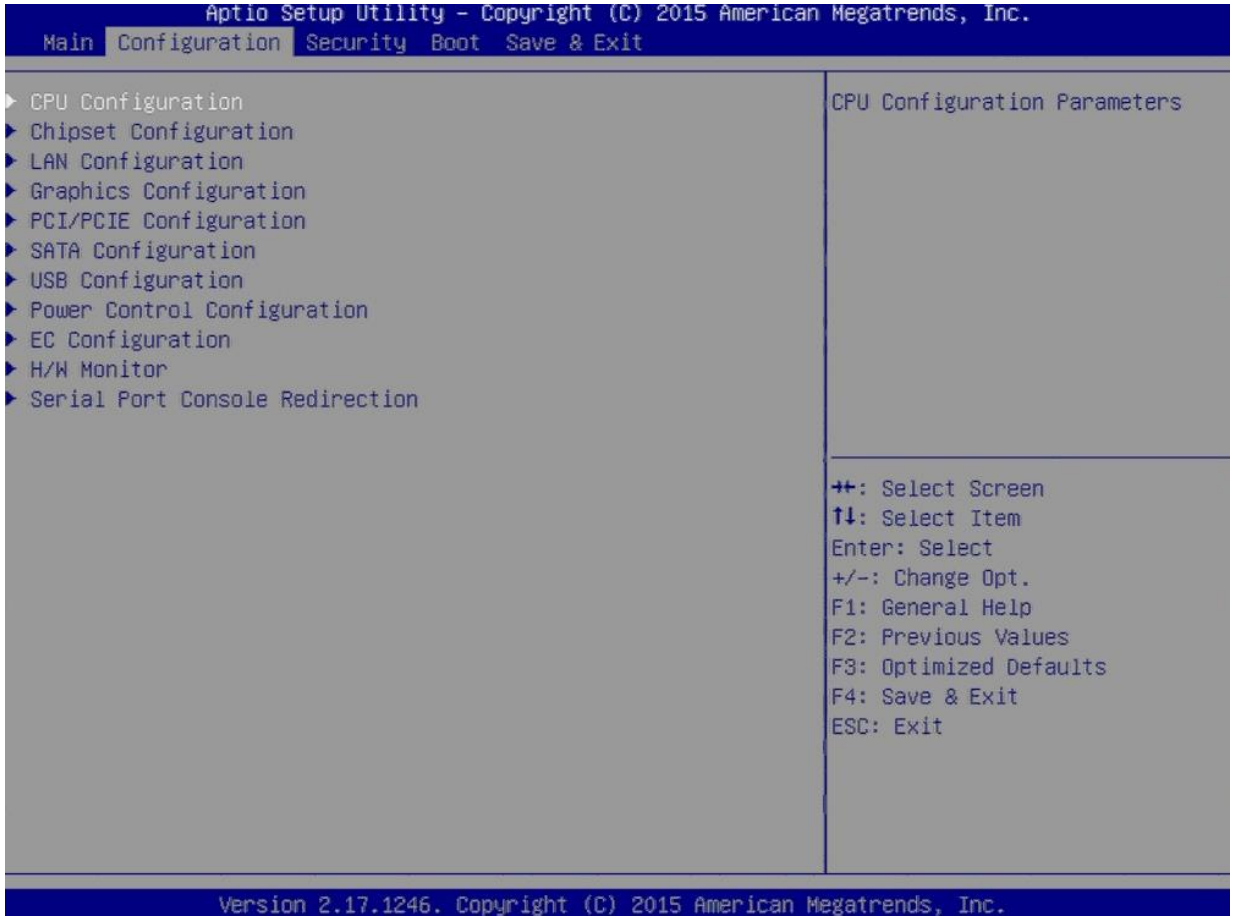
Use this menu for basic system configurations, such as time, date etc.



Feature	Description	Options
System Date	The date format is <Day>, <Month><Date><Year>. Use [+] or [—] to configure system Date.	
System Time	The time format is <Hour><Minute><Second>. Use [+] or [—] to configure system Time.	

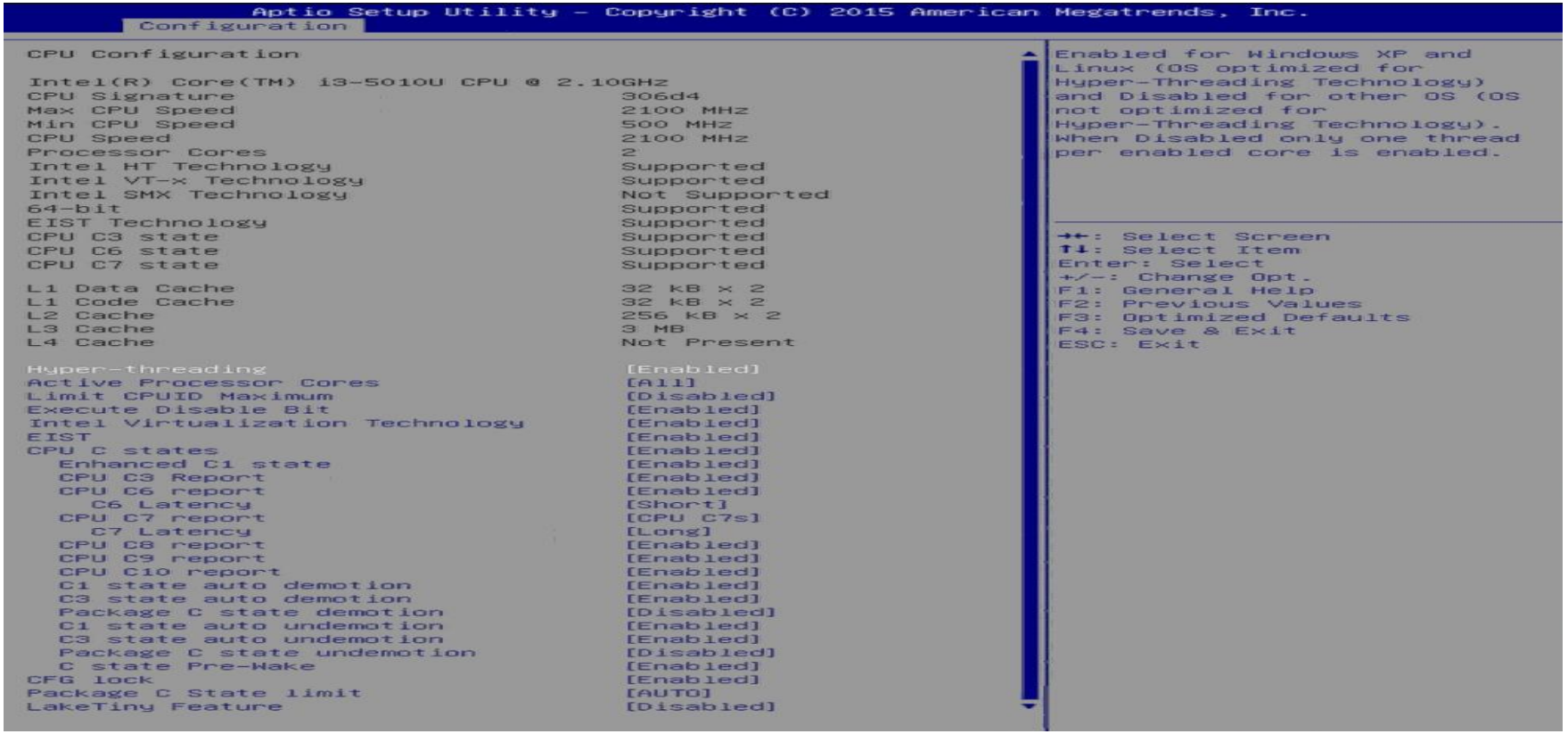
7.2.2 Configuration

Use this menu to set up the items of special enhanced features



CPU Configuration

CPU Configuration Parameters

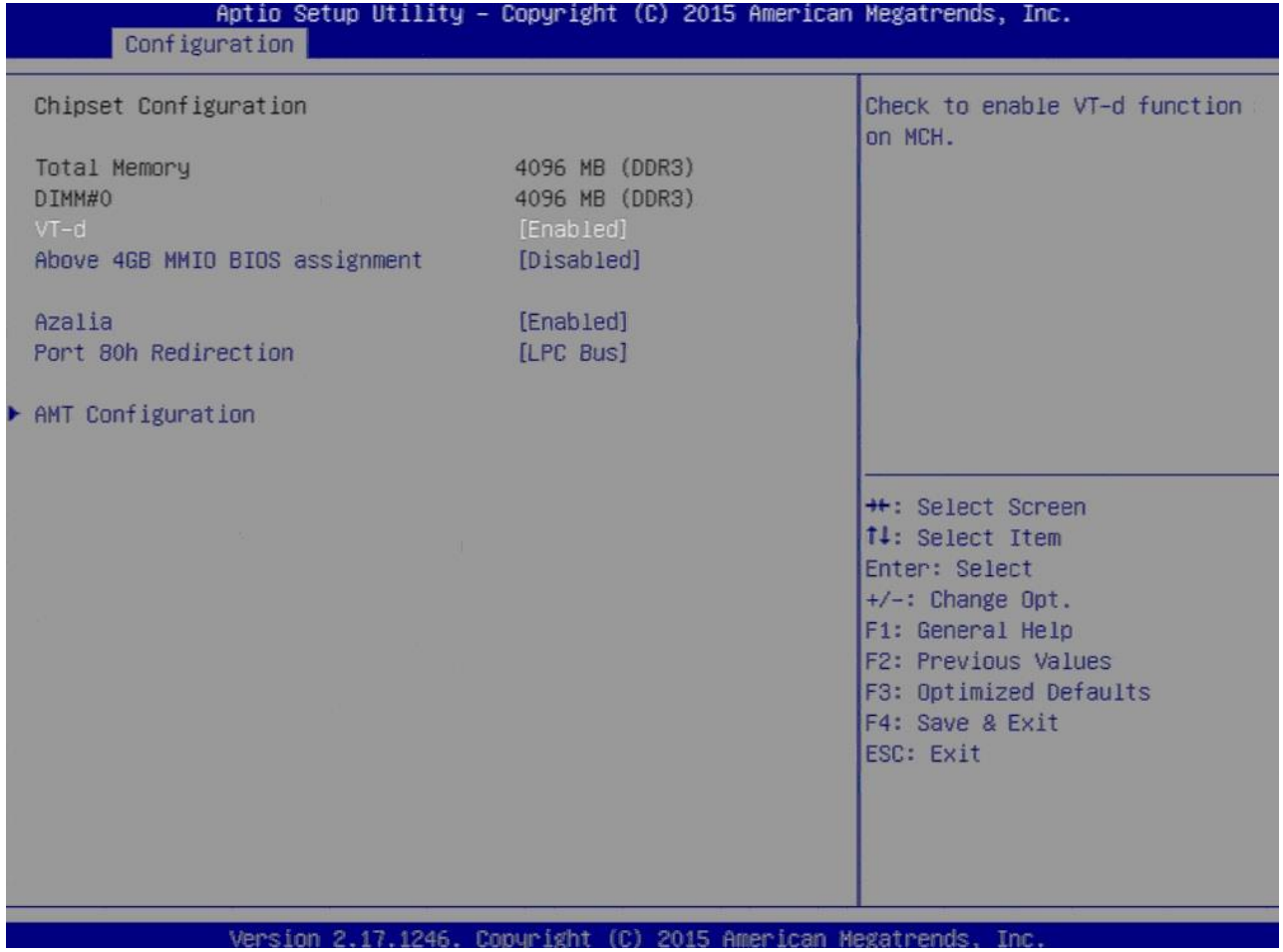


Feature	Description	Options
Hyper-Threading	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.	Disabled, ★Enabled
Active Processor Cores	Number of cores to enable in each processor package.	★All, 1
Limit CPUID Maximum	Disabled for Windows XP	★Disabled, Enabled
Execute Disable Bit	XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.)	Disabled, ★Enabled
Intel Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vander pool Technology	Disabled, ★Enabled
EIST	Enabled/ Disabled Intel Speedstep	Disabled, ★Enabled
CPU C states (Enabled)	Enable or disable CPU C state	★Disabled, Enabled
Enhanced C1 state	Enhanced C1 state	Disabled, ★Enabled
CPU C3 Report	Enable/ Disable CPU C3 report to OS	Disabled, ★Enabled
CPU C6 Report	Enable/ Disable CPU C6 report to OS	Disabled, ★Enabled
C6 Latency	Configure Short/Long latency for C6	★Short, Long
CPU C7 report	Enable/Disable CPU C7 report to OS	Disabled, CPU C7, ★CPU C7s
C7 Latency	Configure Short/Long latency for C7	Short, ★Long
CPU C8 report	Enable/Disable CPU C8 report to OS	Disabled, ★Enabled
CPU C9 report	Enable/Disable CPU C9 report to OS	Disabled, ★Enabled
CPU C10 report	Enable/Disable CPU C10 report to OS	Disabled, ★Enabled

C1 state auto demotion	Processor will conditionally demote C3/C6/C7 requests to C1 based on uncore auto-demote information	Disabled, ★Enabled
C3 state auto demotion	Processor will conditionally demote C6/C7 requests to C3 based on uncore auto-demote information	Disabled, ★Enabled
Package C state demotion	Enable Package C state demotion.	★Disabled, Enabled
C1 state auto un-demotion	Un-demotion from Demoted C1.	Disabled, ★Enabled
C3 state auto un-demotion	Un-demotion from Demoted C3.	Disabled, ★Enabled
Package C state un-demotion	Enable Package C state un-demotion.	★Disabled, Enabled
C state Pre-Wake	Enable or disable C state Pre-Wake feature.	Disabled, ★Enabled
CFG lock	Configure MSR 0xE2[15], CFG lock bit.	Disabled, ★Enabled
Package C State limit	Package C State limit	C0, C2, C3, C6, C7, C7s, C8, C9, C10, ★AUTO
LakeTiny Feature	Enable/Disable LakeTiny for C state configuration	★Disabled, Enabled

Chipset Configuration

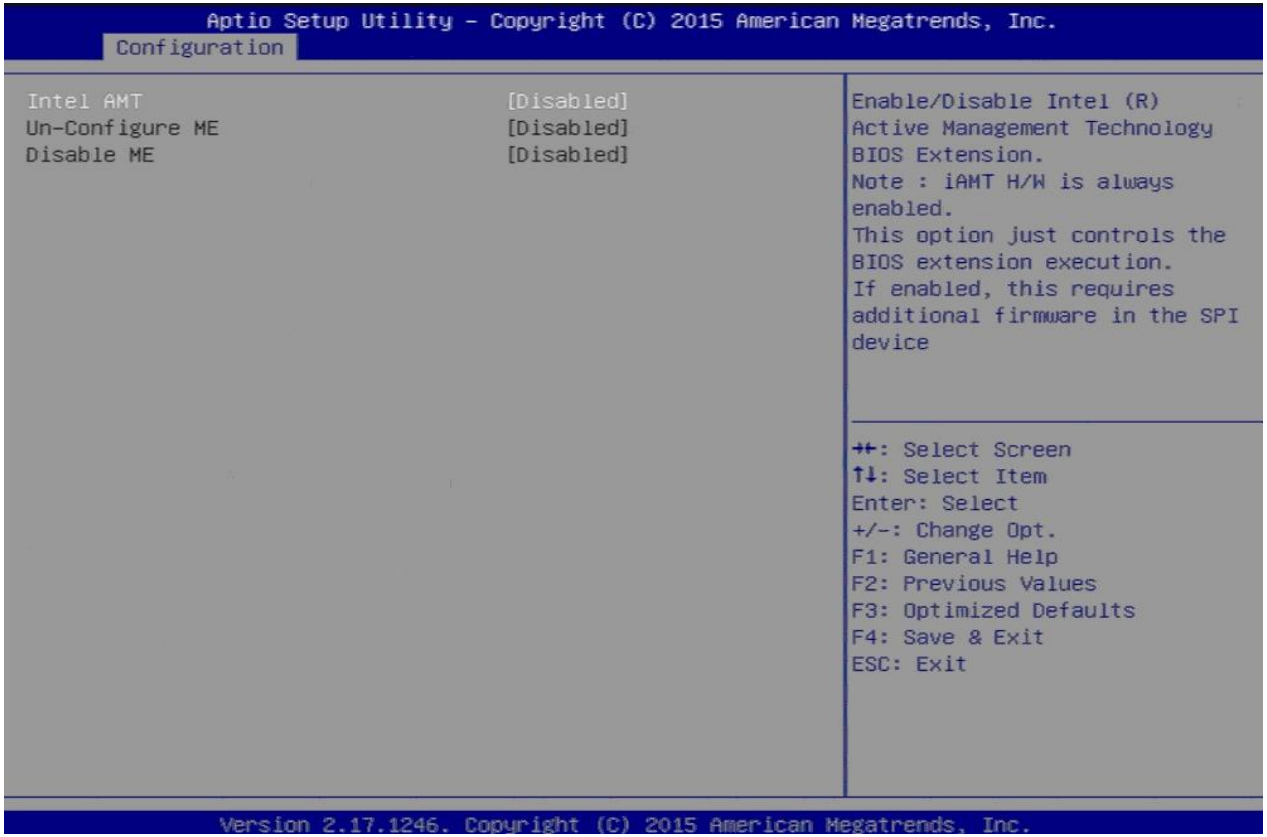
Configure Chipset feature



Feature	Description	Options
VT-d	Check to enable VT-d function on MCH	Disabled, ★Enabled
Above 4GB MMIO BIOS assignment	Enabled/Disabled above 4GB Memory MappedIO BIOS assignment.	Enabled, ★Disabled
Azalia	Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled Enabled = Azalia will be unconditionally enabled	★Enabled, Disabled
Port 80h Redirection	Control where the Port 80h cycles are sent.	★LPC Bus, PCIE Bus

AMT Configuration

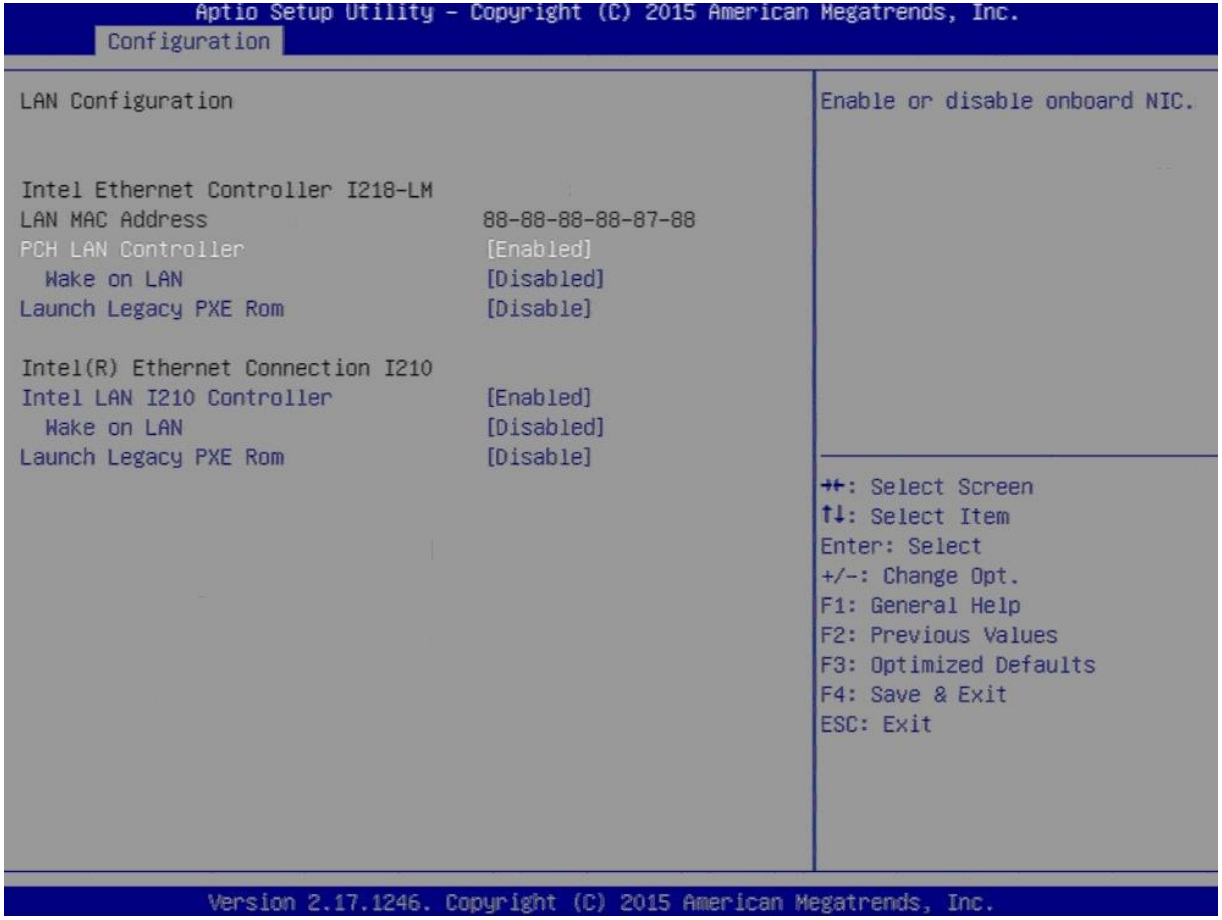
Configure Active Management Technology Parameters



Feature	Description	Options
Intel AMT (Enable)	Enable/Disable Intel® Active Management Technology BIOS Extension. Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device	★Disabled, Enabled
Un-Configure ME	OEMFlag Bit 15:Un-Confugure ME without password	★Disabled, Enabled
Disable ME	Set ME to Soft Temporary Disabled.	★Disabled, Enabled

LAN Configuration

Configuration Onboard LAN device



Feature	Description	Options
PCH LAN Controller	Enable or disable onboard NIC.	★Enabled, Disabled
Wake on LAN	Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)	Enabled, ★Disabled
Launch Legacy PXE Rom	Launch Legacy PXE Rom. [Disable] Not launch Rom, [Enable] Force launch Rom, [Auto] Auto detect LAN cable status to Enable/Disable Rom initial	★Disable, Enable, Auto
Intel LAN I210 Controller	Enable or disable Intel LAN I210	Disabled, ★Enabled
Wake on LAN	Enable or disable integrated LAN to wake the system. (The Wale On LAN cannot be disabled if ME is on at Sx state.)	Enabled, ★Disabled
Launch Legacy PXE Rom	Launch Legacy PXE Rom. [Disable] Not launch Rom, [Enable] Force launch Rom, [Auto] Auto detect LAN cable status to Enable/Disable Rom initial	★Disable, Enable, Auto

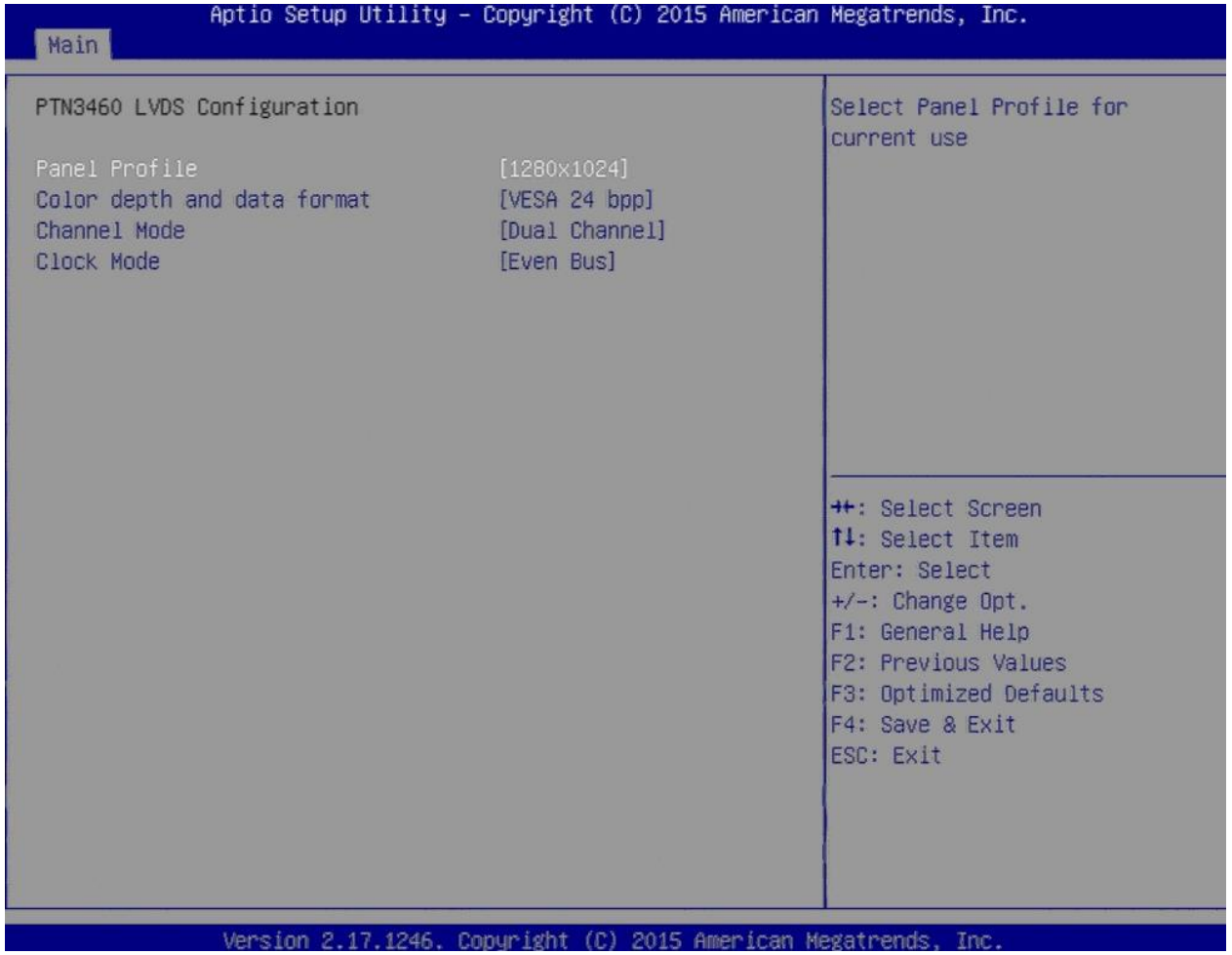
Graphics Configuration

Configuration Graphic Settings

Feature	Description	Options
Internal Graphics	Keep IGD enabled based on the setup options.	★Auto, Disabled, Enabled
DVMT Pre-Allocated	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.	★32M, 64M, 96M, 128M,160M, 192M,,224M, 256M, 288M, 320M ,352M, 384M, 416M,448M, 480M, 512M, 1024M, 2016M
DVMT Total Gfx Mem	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphic Device.	128M, ★256M, MAX
Primary IGFX Boot Display	Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection.	★VBIOS Default, Mini DP Port1, Mini DP Port2, LVDS
Active LFP	Select the Active LFP Configuration. No LVDS: VBIOS does not enable LVDS. eDP Port-A:LFP Driven by Int-DisplayPort encoder from Port-A (eDP to PTN3460 LVDS)	No LVDS, ★eDP Port-A

PTN3460 LVDS Configuration

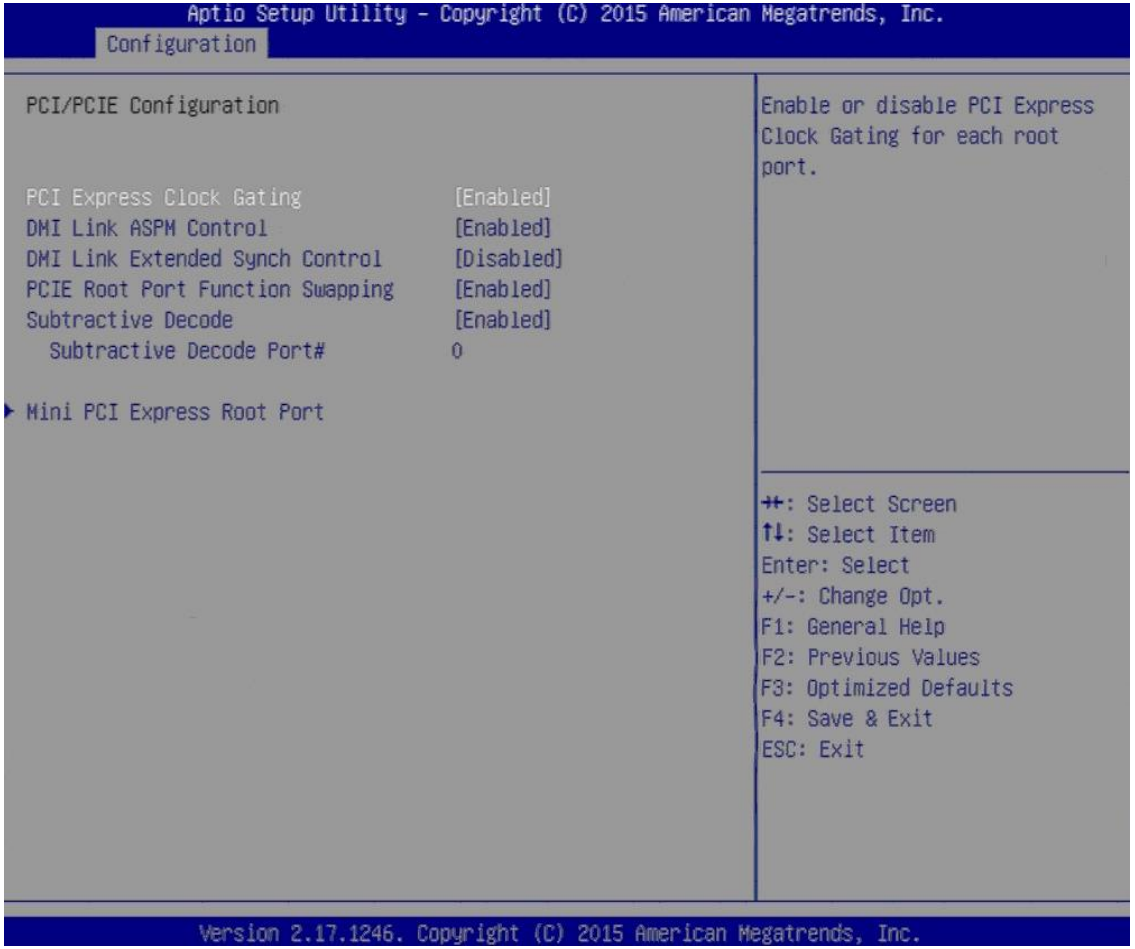
PTN3460 LVDS Help



Feature	Description	Options
Panel Profile	Select Panel Profile for current use	640x480, 800x480, 800x600, 1024x768, 1280x800, ★1280x1024, 1366x768, 1440x900, 1920x1080
Color depth and data format	Select color depth and data format.	★VESA 24 bpp, JEIDA 24 bpp, VESA and JEIDA 18 bpp
Channel Mode	Select LVDS Channel Mode	Single Channel, ★Dual Channel
Clock Mode	Select clock output for LVDS	★Even Bus, Odd Bus, Both Buses

PCI/PCIE Configuration

PCI, PCI-X and PCI Express Settings.



Feature	Description	Options
PCI Express Clock Gating	Enable or disable PCI Express Clock Gating for each root port.	Disabled, ★Enabled
DMI Link ASPM Control	The control of Active State Power Management on both NB side and SB side of the DMI Link.	Disabled, ★Enabled
DMI Link Extended Synch Control	The control of Extended Synch on SB side of the DMI Link.	★Disabled, Enabled
PCIE Root Port Function Swapping	Enable or Disable PCI Express PCI Express Root Port Function Swapping.	Disabled, ★Enabled
Subtractive Decode (Enabled)	Enable or disable PCI Express Subtractive Decode.	★Disabled, Enabled
Subtractive Decode Port#	Select PCI Express Subtractive Decode Root Port. User to ensure port availability	

Mini PCI Express Root Port

Mini PCI Express Root Port Settings

Feature	Description	Options
PCI Express Root Port	Control the PCI Express Root Port.	Disabled, ★Enabled
ASPM	PCI Express Active State Power Management settings.	★Disabled, L0s, L1, L0sL1, Auto
PCIe Speed	Select PCI Express port speed.	★Auto, Gen 1, Gen 2

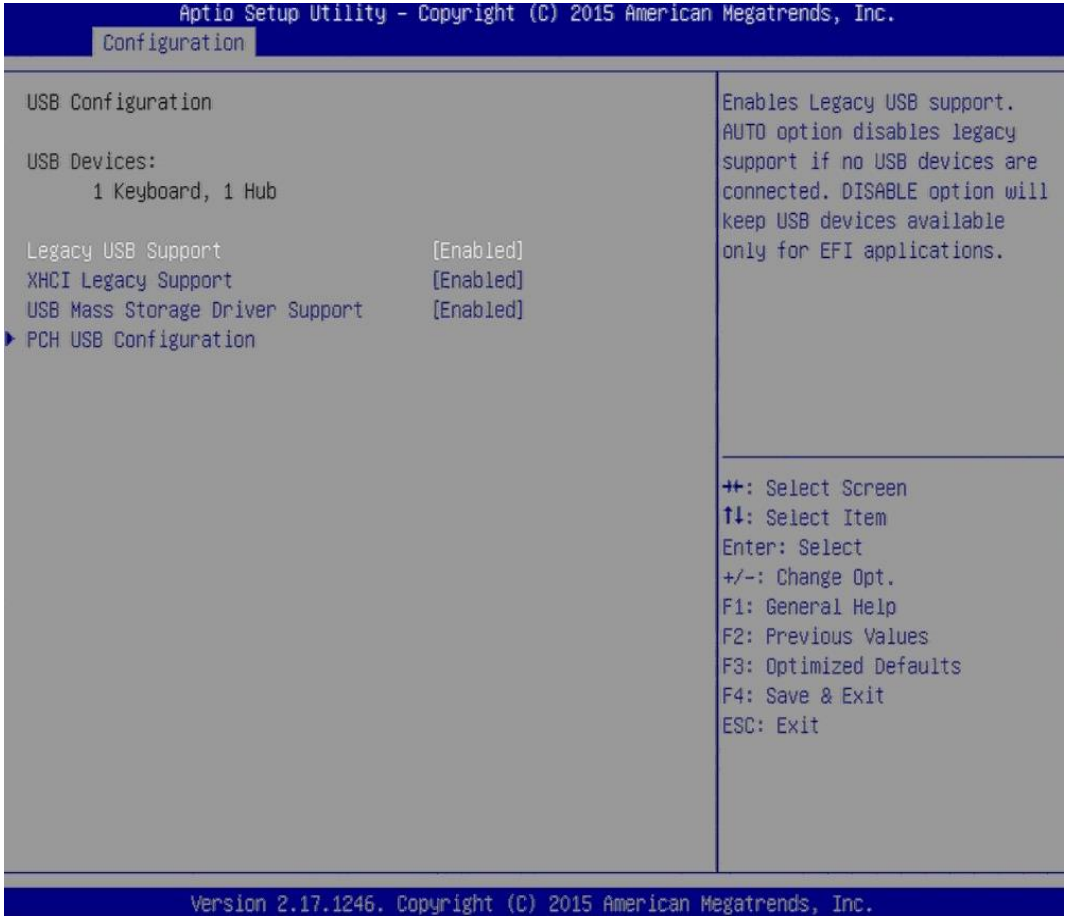
SATA Configuration

SATA Device Options Settings

Feature	Description	Options
SATA Controller(s)	Enable or Disable SATA Device.	★Enabled, Disabled
SATA Mode Selection	Determines how SATA controller(s) operate.	★AHCI
SATA Controller Speed	Indicates the maximum speed the SATA controller can support.	★Default, Gen1, Gen2, Gen3
Port 0	Enable or Disable SATA Port	Disabled, ★Enabled
Hot plug (Enabled)	Designates this port as Hot Pluggable.	★Disabled, Enabled
Mechanical Presence Switch	Controls reporting if this port has a Mechanical Presence Switch. Note: Requires hardware support.	★Disabled, Enabled
External SATA	External SATA Support.	★Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	★Hard Disk Drive, Solid State Drive
Port 1	Enable or Disable SATA Port	Disabled, ★Enabled
Hot Plug (Enabled)	Designates this port as Hot luggable.	★Disabled, Enabled
Mechanical presence Switch	Controls reporting if this port has a Mechanical Presence Switch. Note: Requires hardware support.	★Disabled, Enabled
External SATA	External SATA Support.	★Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	★Hard Disk Drive, Solid State Drive

USB configuration

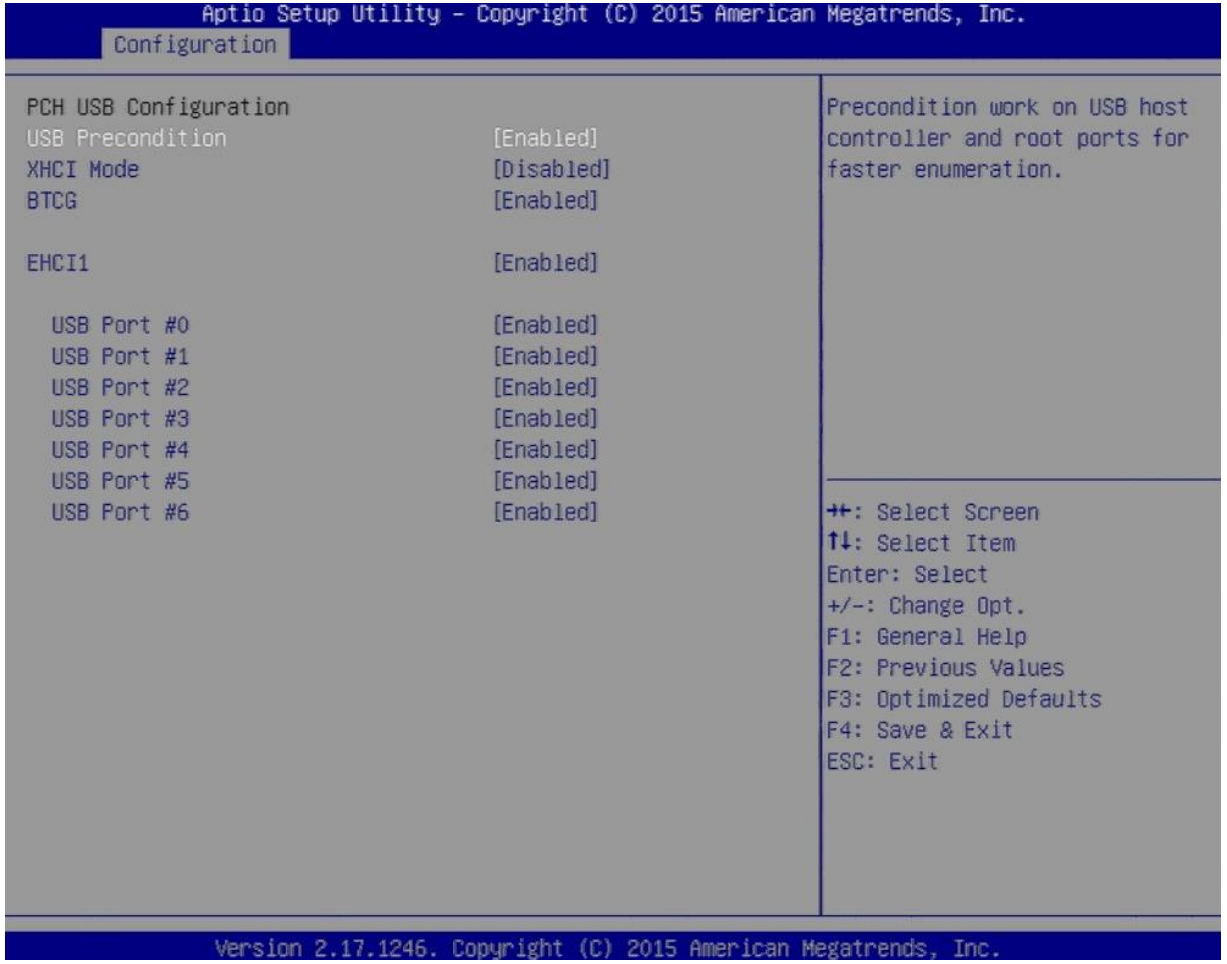
USB Configuration Parameters



Feature	Description	Options
Legacy USB Support	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.	★Enabled, Disabled, Auto
XHCI Legacy Support	Enable/Disable XHCI Controller Legacy support.	★Enabled, Disabled
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support.	Disabled, ★Enabled

PCH USB Configuration

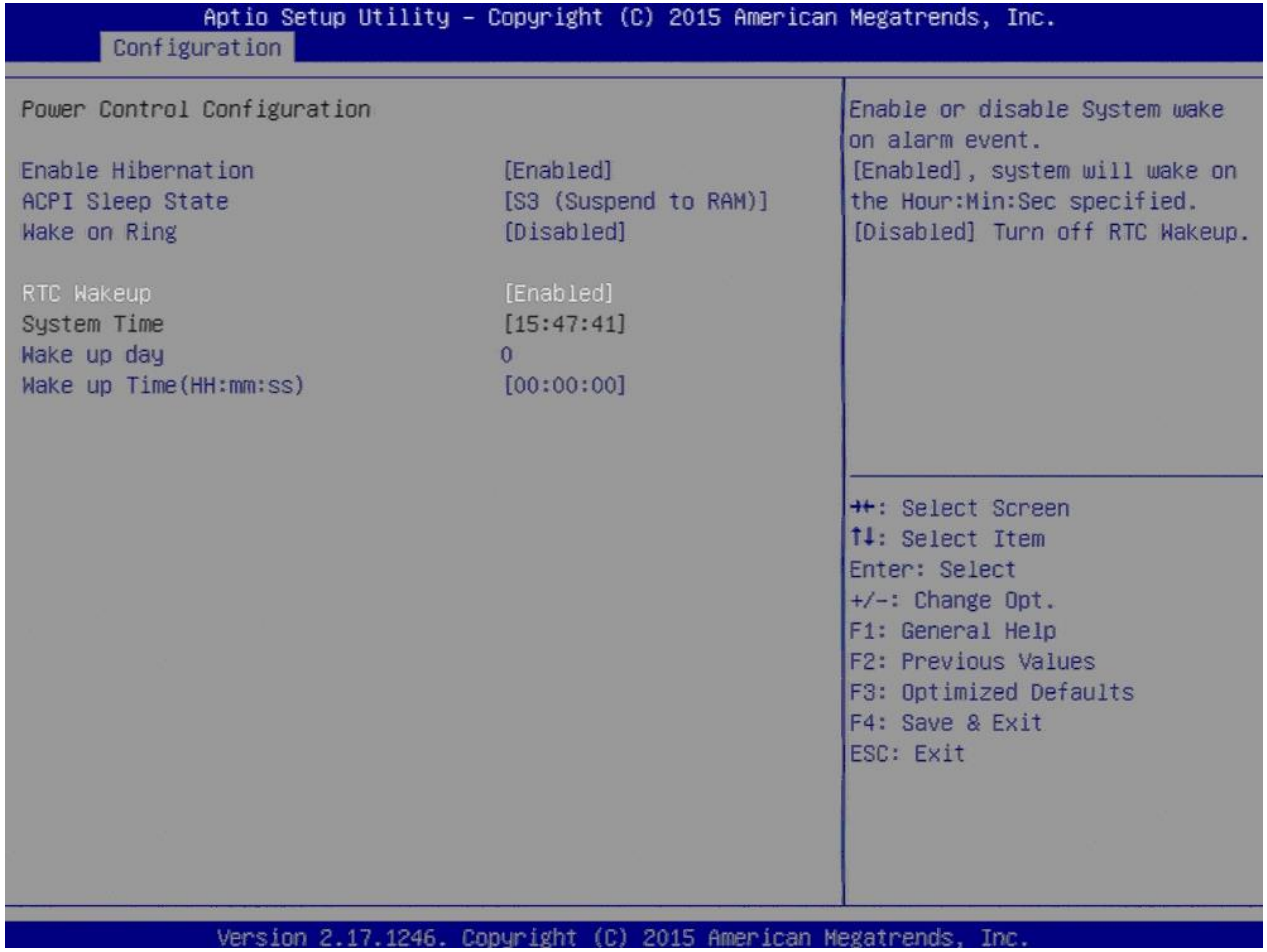
PCH USB Configuration



Feature	Description	Options
USB Precondition	Precondition work on USB host controller and root ports for faster enumeration.	Disabled, ★Enabled
XHCI Mode	Mode of operation of xHCI controller.	★Smart Auto, Auto, Enabled, Disabled
BTCG	Enabling/disabling trunk clock gating.	★Enabled, Disabled
USB Port #0	Enable / Disable USB port.	Disabled, ★Enabled
USB Port #1	Enable / Disable USB port.	Disabled, ★Enabled
USB Port #2	Enable / Disable USB port.	Disabled, ★Enabled
USB Port #3	Enable / Disable USB port.	Disabled, ★Enabled
USB Port #4	Enable / Disable USB port.	Disabled, ★Enabled
USB Port #5	Enable / Disable USB port.	Disabled, ★Enabled
USB Port #6	Enable / Disable USB port.	Disabled, ★Enabled

Power Control Configuration

System Power Control Configuration Parameters



Feature	Description	Options
Enable Hibernation	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.	Disabled, ★Enabled
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.	Suspend Disabled, ★S3(Suspend to RAM)
Wake on Ring	Enable/Disable GPIO Wake On Ring function.	★Disabled, Enabled
RTC Wakeup (Enabled)	Enable or disable System wake on alarm event. [Enabled], system will wake on the hr::min::sec specified. [Disabled] Turn off RTC Wakeup.	★Disabled, Enabled
Wake up day	Select 0 for daily system wake up 1-31 for which day of the month that you would like the system to wake up	0-31
Wake up Time (HH:mm:ss)	Use [Enter], [TAB] to select field, HH: 0-23 mm: 0-59 ss: 0-59	HH: 0-23 mm: 0-59 ss: 0-59

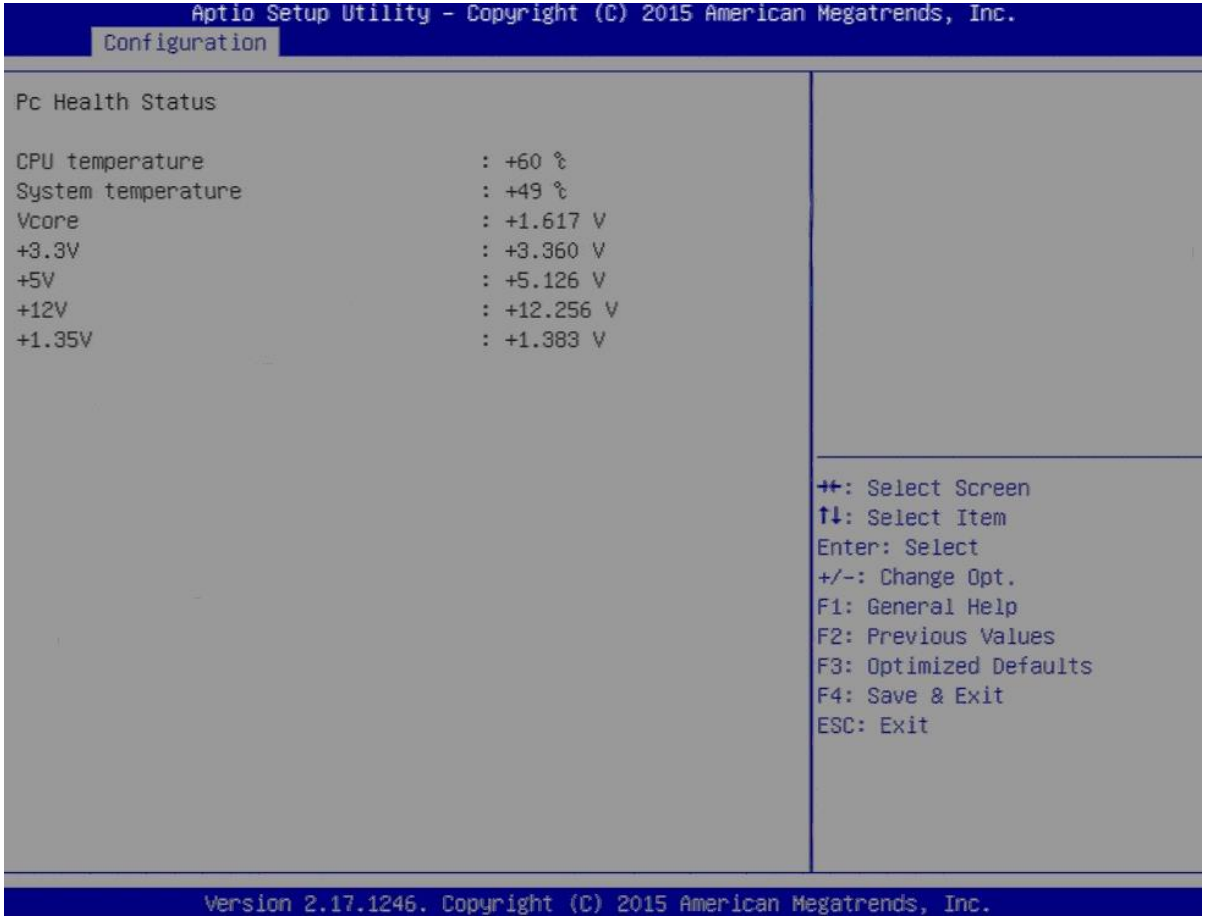
EC Configuration

System EC Chip Parameters

Feature	Description	Options
Serial Port 1	Enable or Disable Serial Port (COM)	Disabled, ★Enabled
UART Mode	Set Current UART MODE RS232, RS485, RS485/RS422	★RS232, RS485 HALF DUFLEX, RS485/422 FULL DUFLEX
Watch Dog Timer (Enabled)	Enable/Disable Watch Dog Timer	★Disabled, Enabled
Timer Unit	Select Timer count unit of WDT	★Second, Minute
Timer value	Set WDT Timer value seconds/minutes	★20

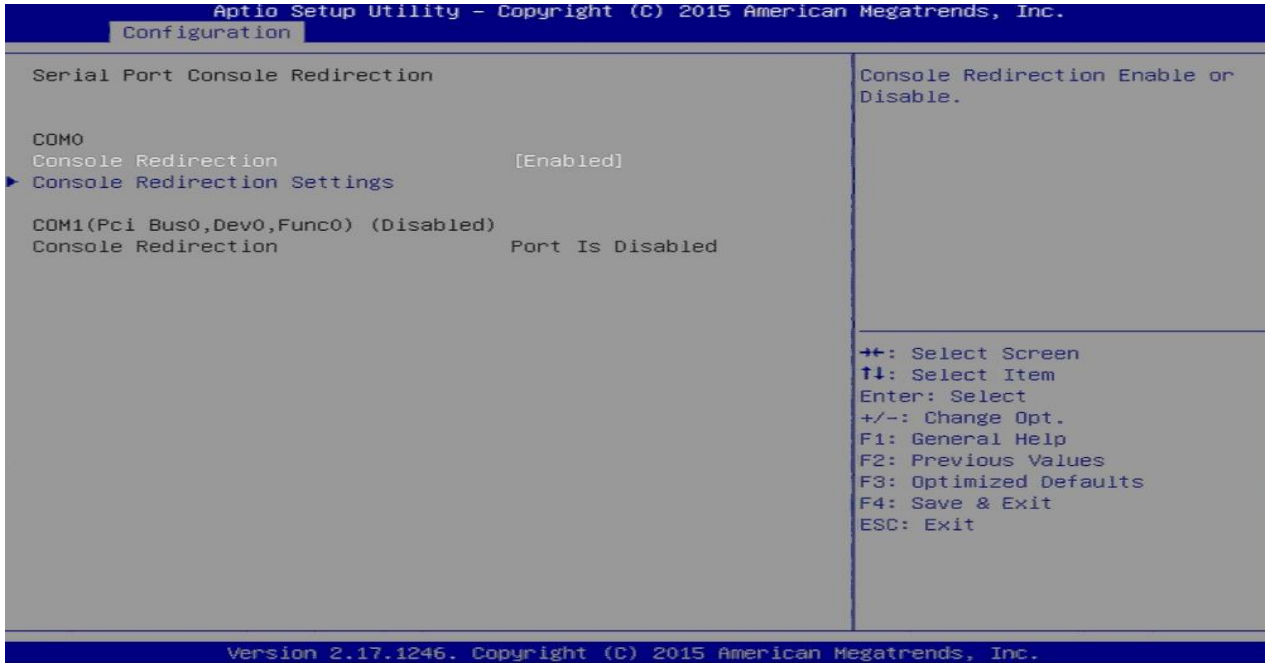
H/W Monitor

Monitor hardware status



Serial Port Console Redirection

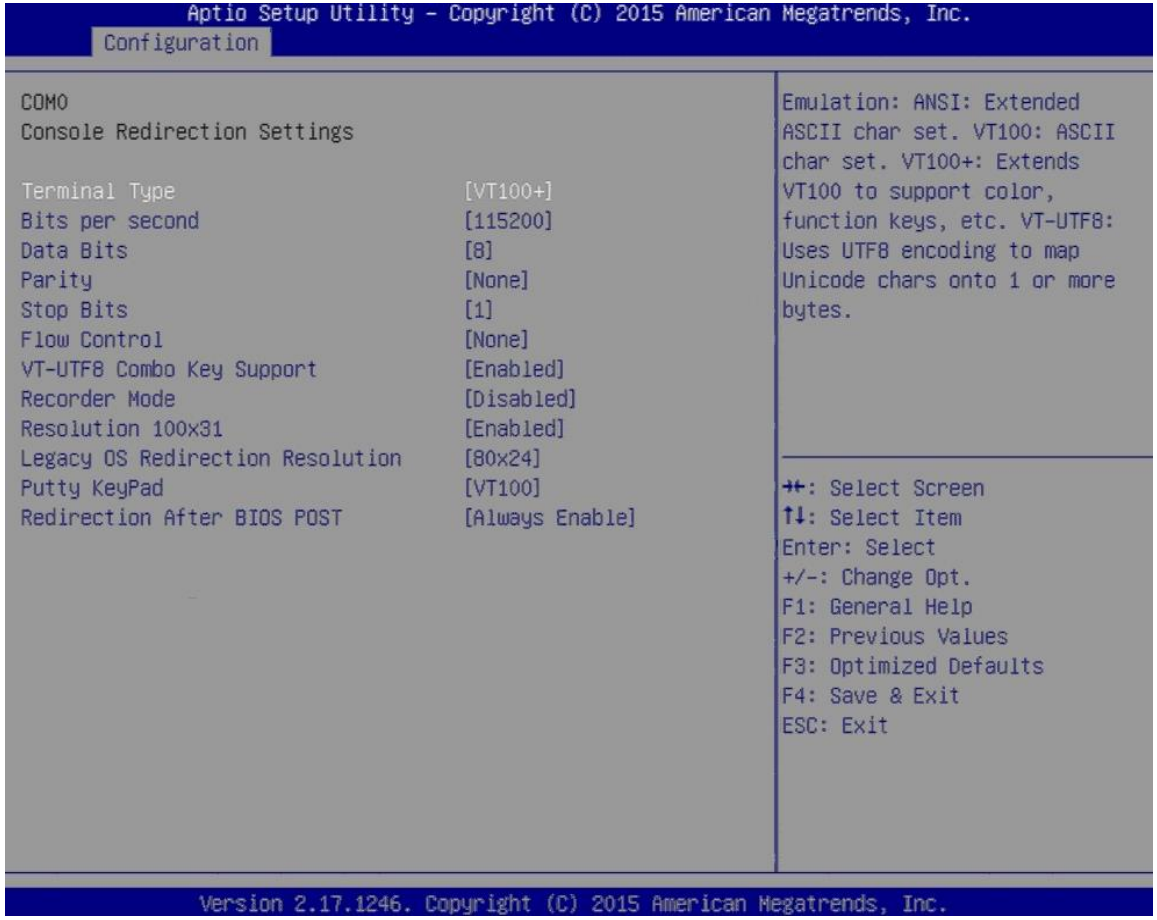
Serial Port Console Redirection



Feature	Description	Options
Console Redirection (Enable)	Console Redirection Enable or Disable.	★Disabled, Enabled

Console Redirection Settings

The settings specify how the host computer and remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

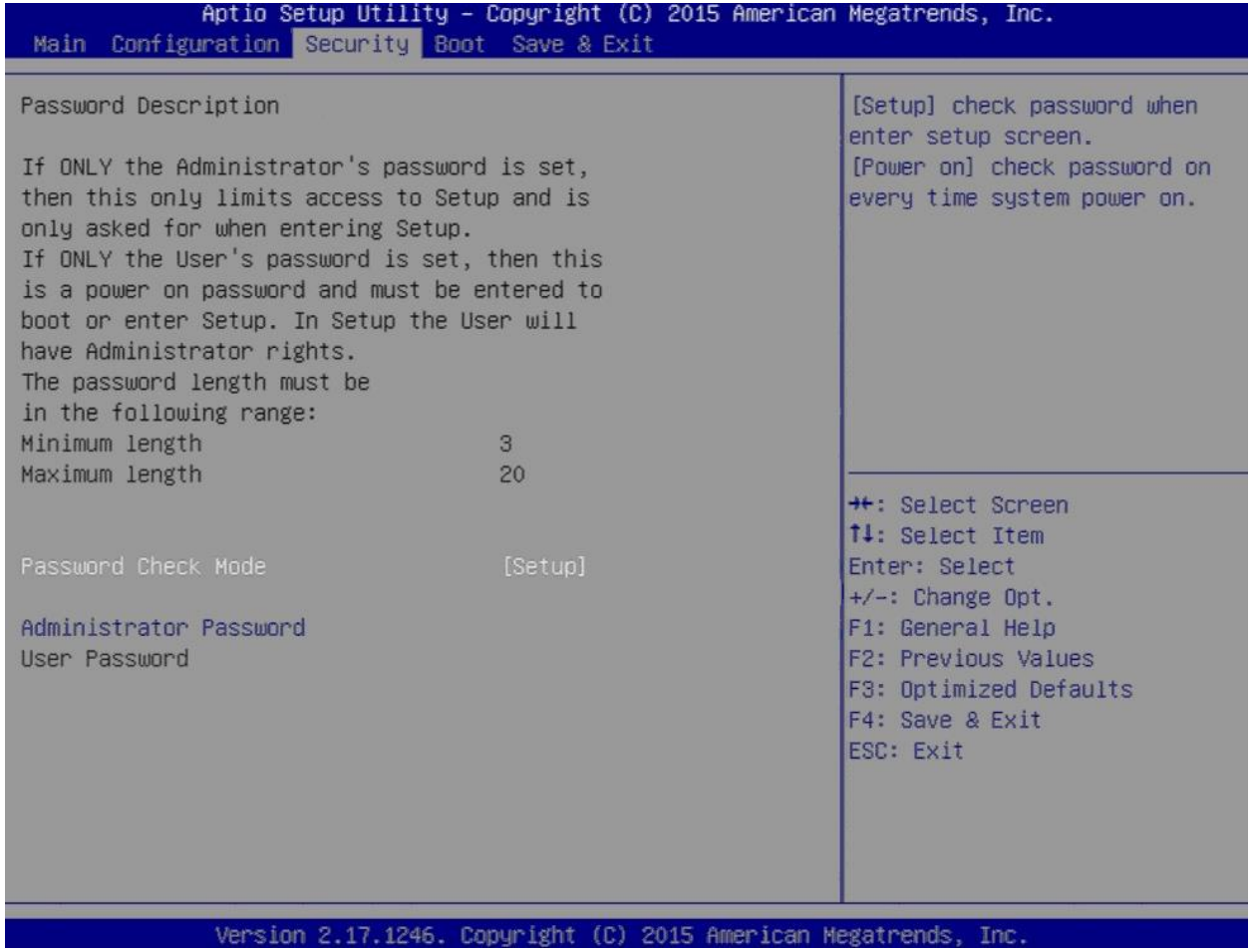


Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes	VT100, ★VT100+, VT-UTF8, ANSI
Bits per second	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.	9600, 19200, 38400, 57600, ★115200
Data Bits	Data Bits	7, ★8
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 is the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	★None, Even, Odd, Mark, Space
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★1,2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	★None, Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	Disabled, ★Enabled
Recorder Mode	With this mode enable only text will be sent. This is to capture Terminal data.	★Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	Disabled, ★Enabled

Legacy OS Redirection Resolution	On Legacy OS, the Number of Rows and Columns supported redirection	★80x24, 80x25
Putty keypad	Select Function Key and Key Pad on Putty.	★VT100, LINUX, XTERM6, SCO, ESCN, VT400
Redirection After BIOS POST	The Setting specify if Boot Loader is selected then Legacy console redirection is disable before booting to Legacy OS. Default value always enable which means Legacy console Redirection is enable for Legacy OS.	★Always Enable, Boot Loader

7.2.3 Security

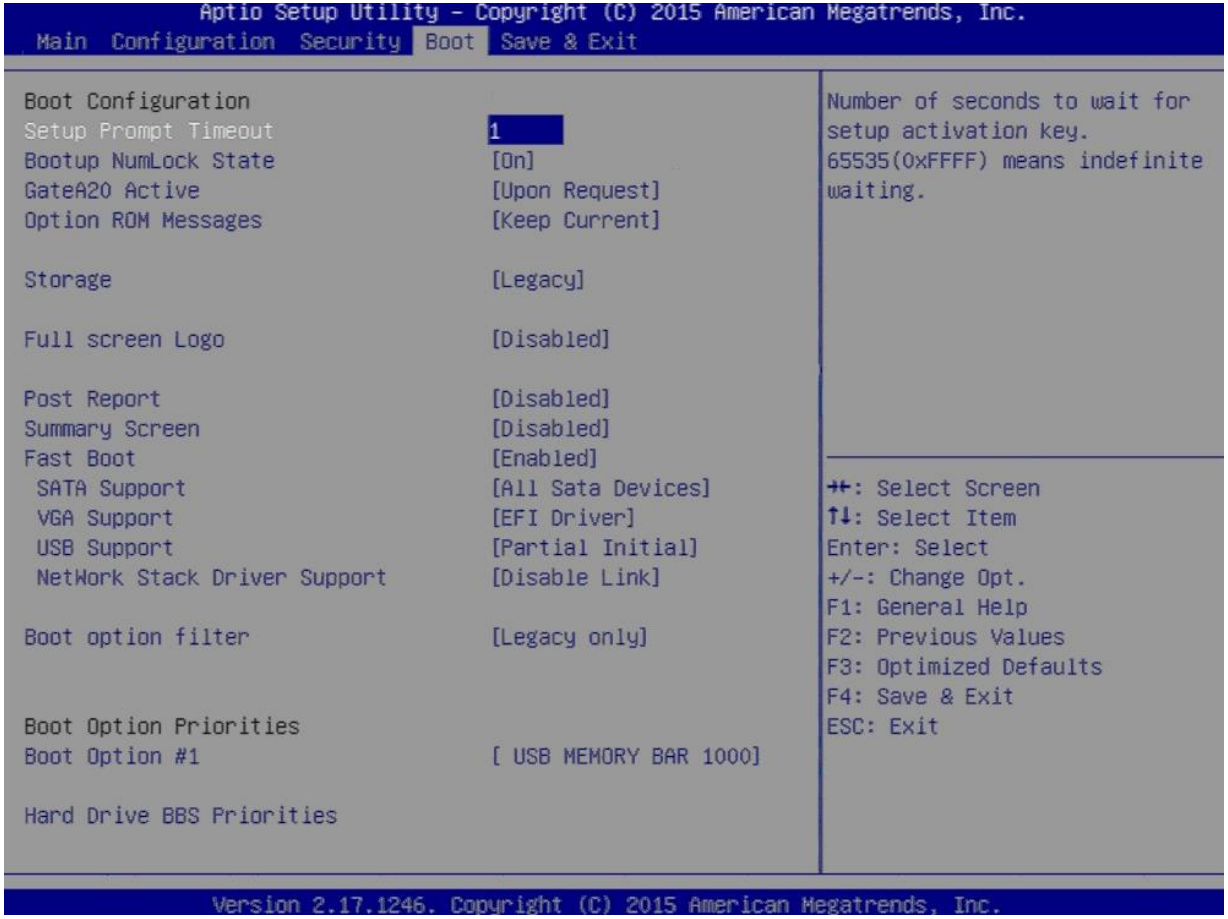
This section lets you set security passwords to control access to the system at boot time and/or when entering the BIOS setup program.



Feature	Description	Options
Password Check Mode	[Setup] check password when enter setup screen. [Power on] check password on every time system power on.	★Setup Power On
Administrator Password	Set Administrator Password	Create New Password

7.2.4 Boot

Use this menu to specify the priority of boot devices.



Feature	Description	Options
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	★1
BootupNumLock State	Select the Keyboard NumLock state	★On, off
GateA20 Active	UPON REQUEST – GA20 can be disabled using BIOS services. ALWAYS- do not allow disabling GA20; this option is useful when any RT code is execute above 1MB	★Upon Request, Always
Option ROM Messages	Set display mode for Option ROM	Force BIOS, ★Keep Current
Storage	Control the execution of UEFI and Legacy Storage OpROM	Do not launch, UEFI, ★Legacy
Full screen Logo	Enables or disables Quiet Boot option and Full screen Logo.	★Disabled, Enabled
Post Report	Post Report Support Enabled/Disabled	★Disabled, Enabled
Summary Screen	Summary Screen Support Enabled/Disabled	★Disabled, Enabled
Fast Boot (Enabled)	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.	★Disable Link, Enabled
SATA Support		Last Boot HDD Only, ★All State Devices
VGA Support	If Auto, only install Legacy OpRom with Legacy OS and logo would NOT be shown during post. Efi driver will still be installed with EFI OS.	Auto, ★EFI Driver

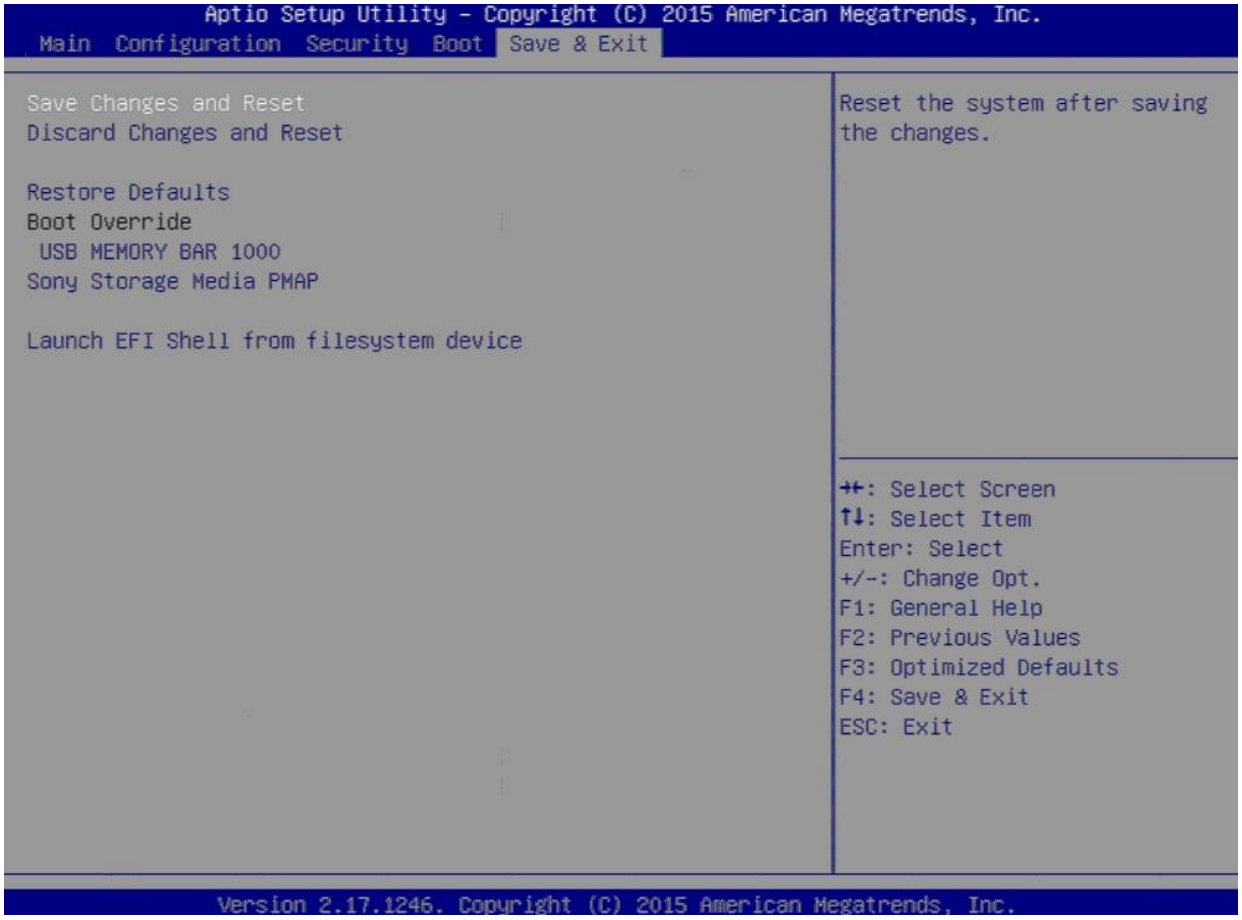
USB Support	If Disabled, all USB devices will NOT be available until after OS boot. If partial Initial, USB Mass Storage and specific USB port/device will NOT be available before OS boot. If Enabled, al USB devices will be available in OS and post.	Disable Link, Full Initial , ★Partial Initial
Network Stack Driver Support	If Disabled, Network Stack Driver will be skipped.	★Disable Link, Enabled
Boot option filter	This option controls Legacy/UEFI ROMs priority	★Legacy only, UEFI only
Boot Option #1	Sets the system boot order	Disabled

Hard Drive BBS Priorities

Set the order of the legacy devices in this group

Feature	Description	Options
Boot Option #1	Sets the system boot order	
Boot Option #2	Sets the system boot order	

7.2.5 Save &Exit



Feature	Description	Options
Save Changes and Reset	Reset the system after saving the changes	
Discard Changes and Reset	Reset system without saving any changes.	
Restore Defaults	Restore/Load Default values for all the setup options.	
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shell.efi) from one of the available filesystem devices	Save configuration and reset? Yes, No

8 Trouble shooting

This section provides a few useful tips to quickly get NANO-6050 running with success. This section will primarily focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

8.1 Hardware Quick Installation

ATX Power Setting

Unlike other Single board computer, NANO-6050 supports ATX 12V 4 Pin or DC 12V Power adaptor only. Therefore, there is no other setting that needs to be setup. However, there is ATX 4 Pin Connector – J10& DC JACK – J1 on the NANO-6050 board.

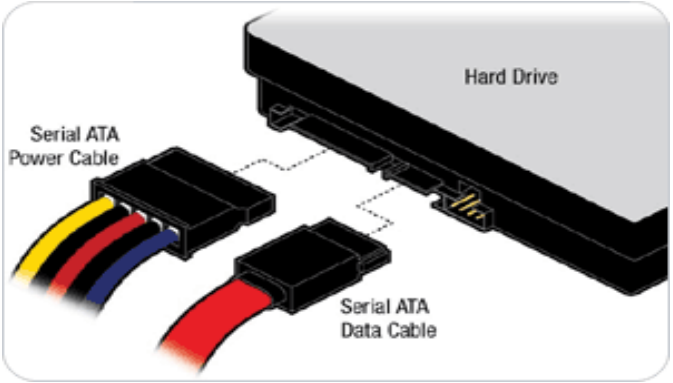
ATX 4 Pin Connector – J10

DC Jack – J

Serial ATA

Unlike IDE bus, each Serial ATA channel can only connect to one SATA hard disk at a time;

The installation of Serial ATA is simpler and easier than IDE, because SATA hard disk doesn't require setting up Master and Slave, which can reduce mistake of hardware installation.



8.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power. 204-pin DDR3L Memory, keyboard, mouse, SATA hard disk, mini DP connector, power cable of the device, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with NANO-6050, it is recommended, when going with the boot-up sequence, to hit “Delete ” or ” Esc” key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to “Restore Defaults”, press “Enter” and select “Yes” to load default optimal BIOS setup. This will force your BIOS setting back to the initial factory configurations. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting at any time when system appears to be unstable in boot up sequence.

8.3 FQA

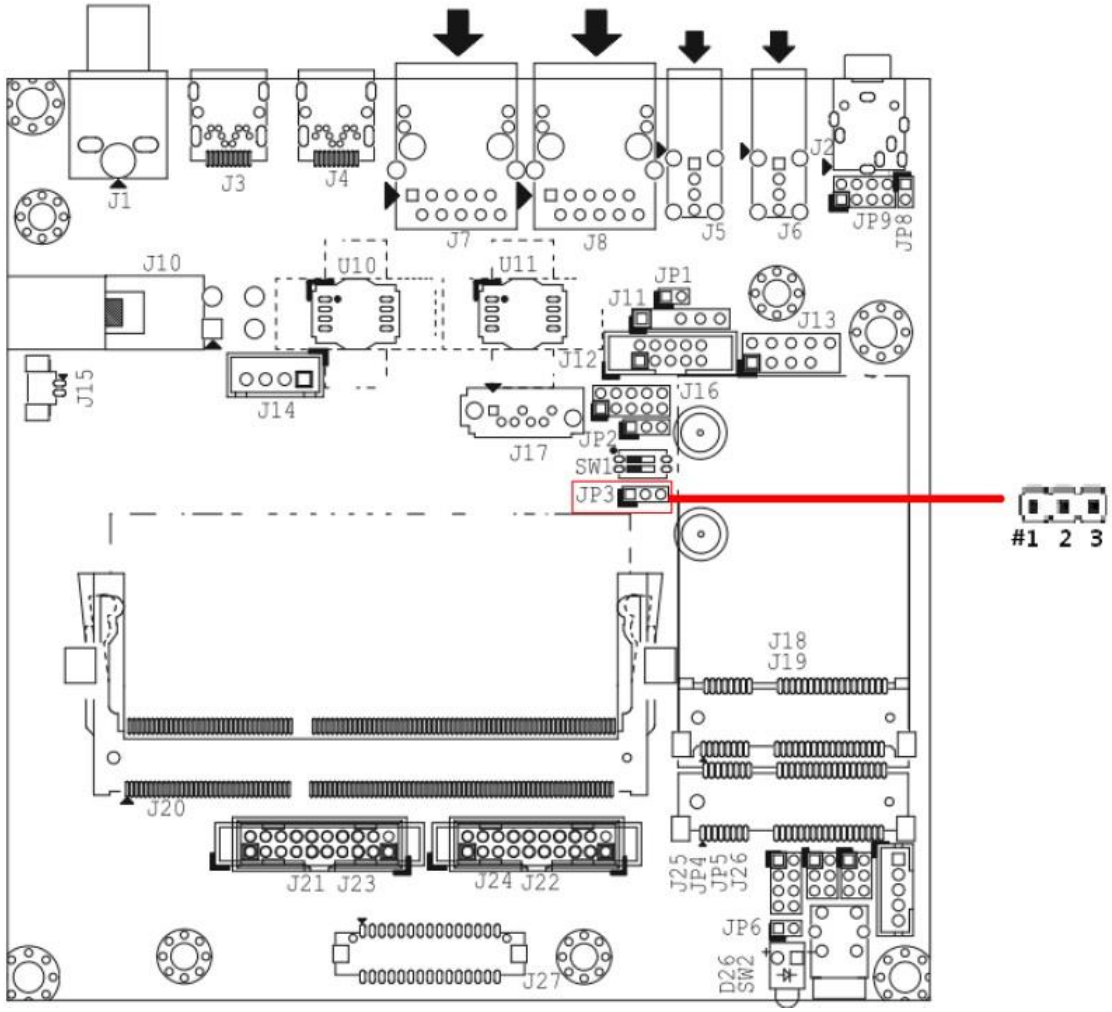
Information & Support

Question: I forgot my password of system BIOS, what am I supposed to do?

Answer: You can switch off your power supply then find the JP3 to set it from 1-2 short to 2-3 short and wait 10 seconds to clean your password then set it back to 1-2 short to switch on your power supply.

JP3：CMOS Setting

	Jumper Setting Describe
*1-2 Short	Normal Operation (Default)
2-3 Short	Clean CMOS


J1
J3
J4
J7
J8
J5
J6
J2
JP9
JP8
J10
U10
U11
JP1
J11
J13
JI2
J15
J14
J16
J17
JP2
SW1
JP3
#1 2 3
J18
J19
J20
J21 J23
J24 J22
J25
JP4
JP5
J26
JP6
D26
SW2
J27

Question:How to update the BIOS file of NANO-6050?

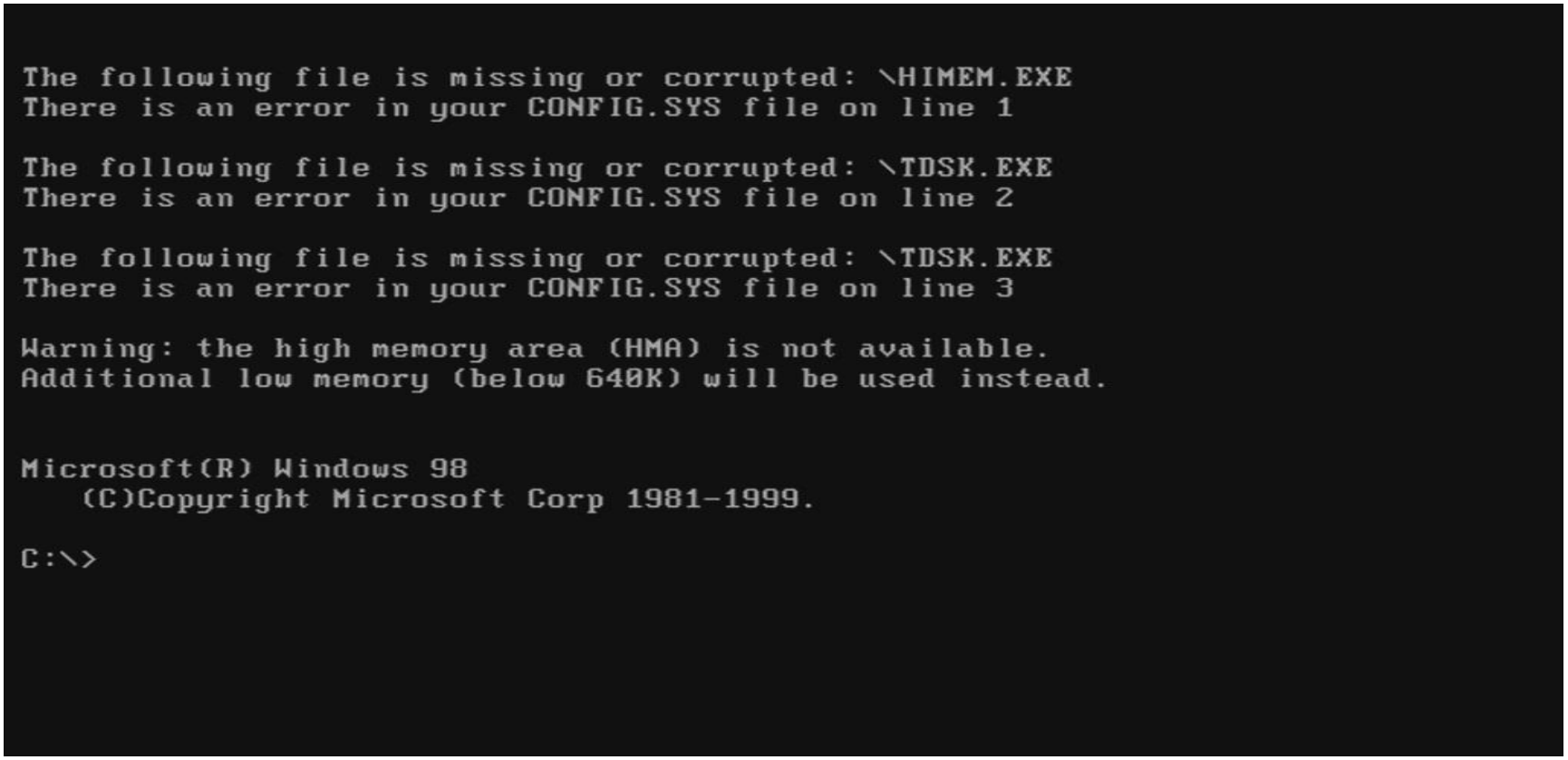
Answer: 1. Please visit web site of **Portwell download center**as below hyperlink

http://www.portwell.com.tw/support/download_center.php

Registering an account in advance is a must. **(The E-Mail box should be an existing Company email address that you check regularly.)**

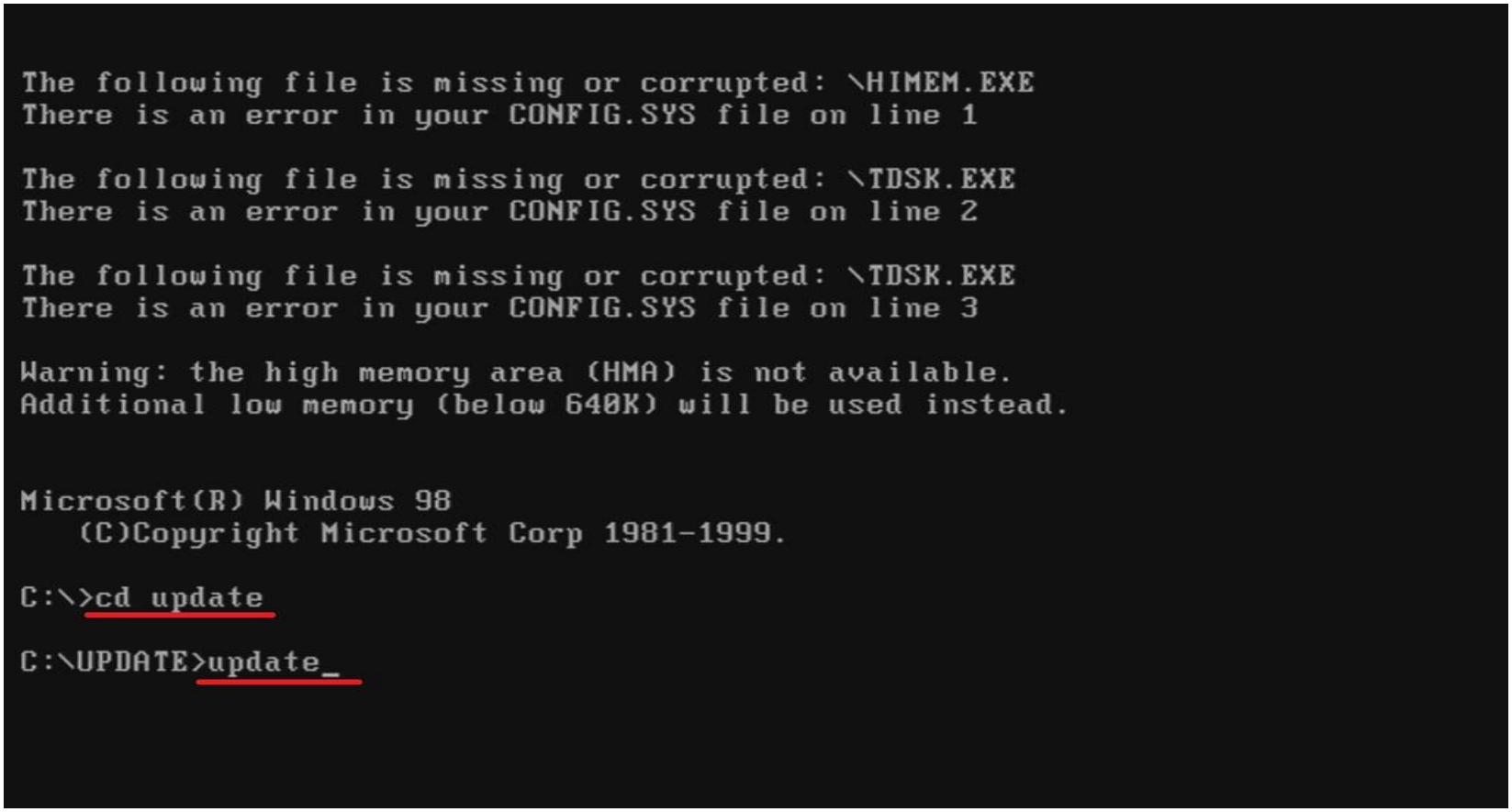
http://www.portwell.com.tw/member/newmember.php

2. Type in your User name and password and log in the download center.
3. Select **"Search download"** and type the keyword **"NANO-6050"**.
4. Find the **"BIOS "**page and download the ROM file and flash utility.
5. Unzip file to bootable USB flash drive which can boot to dos mode. Then execute the **"update.bat"**. It will start to update BIOS.
6. Reboot the system and getting into [DOS]. Please follow the below instruction to update BIOS.

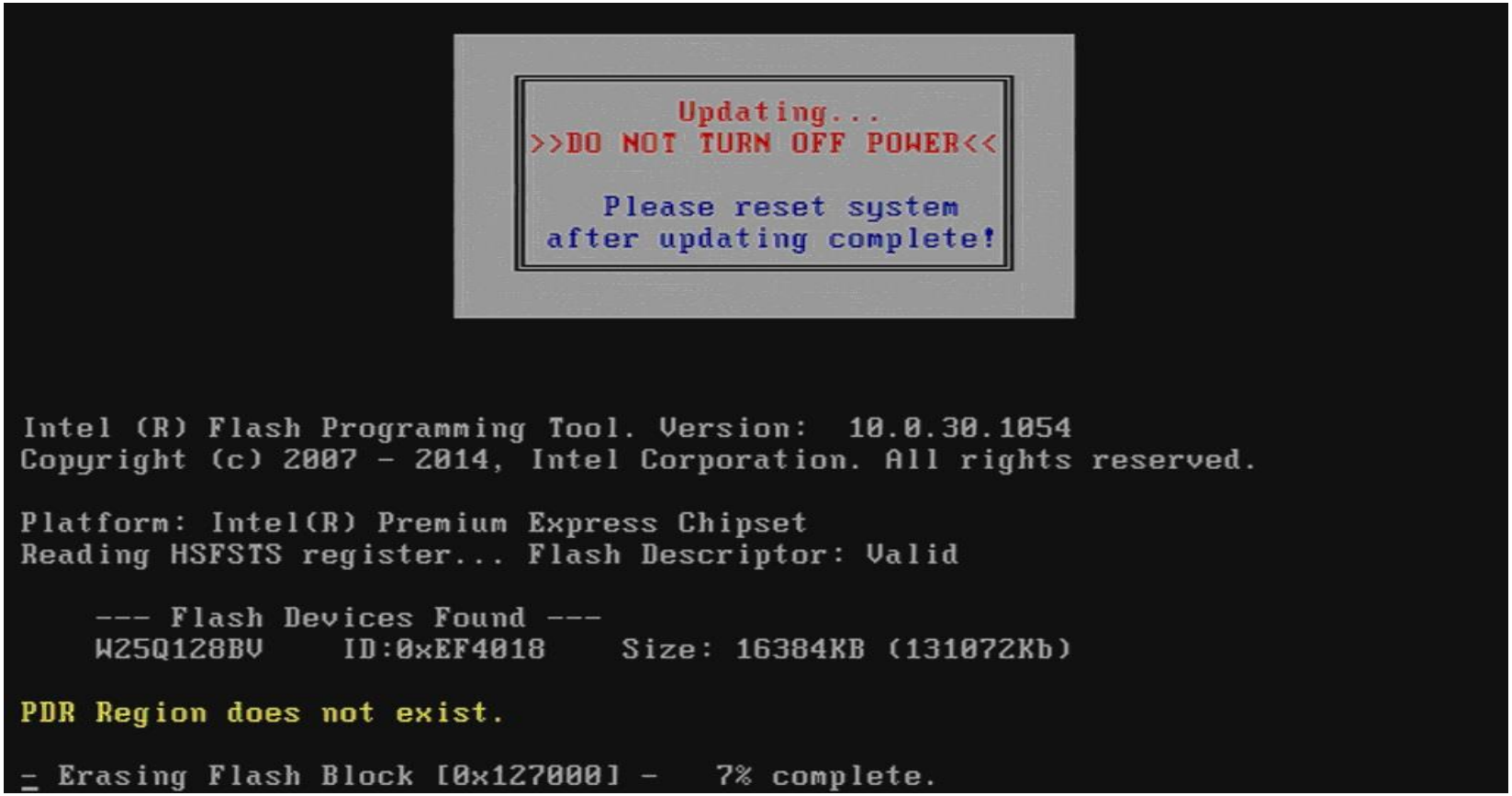

The following file is missing or corrupted: \HIMEM.EXE
There is an error in your CONFIG.SYS file on line 1
The following file is missing or corrupted: \TDSK.EXE
There is an error in your CONFIG.SYS file on line 2
The following file is missing or corrupted: \TDSK.EXE
There is an error in your CONFIG.SYS file on line 3
Warning: the high memory area (HMA) is not available.
Additional low memory (below 640K) will be used instead.
Microsoft(R) Windows 98
(C)Copyright Microsoft Corp 1981-1999.
C:\>

a. “**cd update**” to access the root folder.

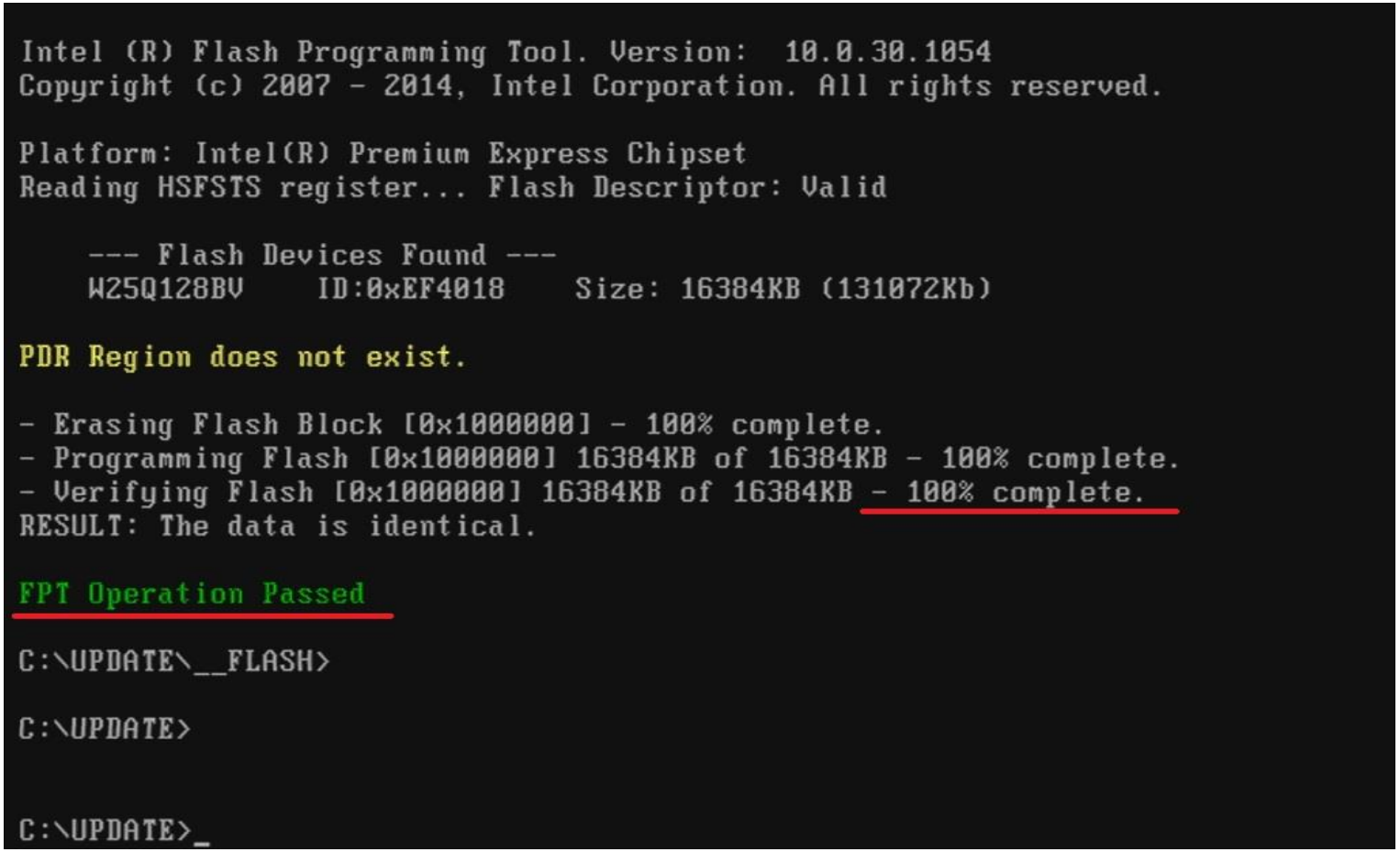
b. Key-in”**update**” this command to run updating procedure.



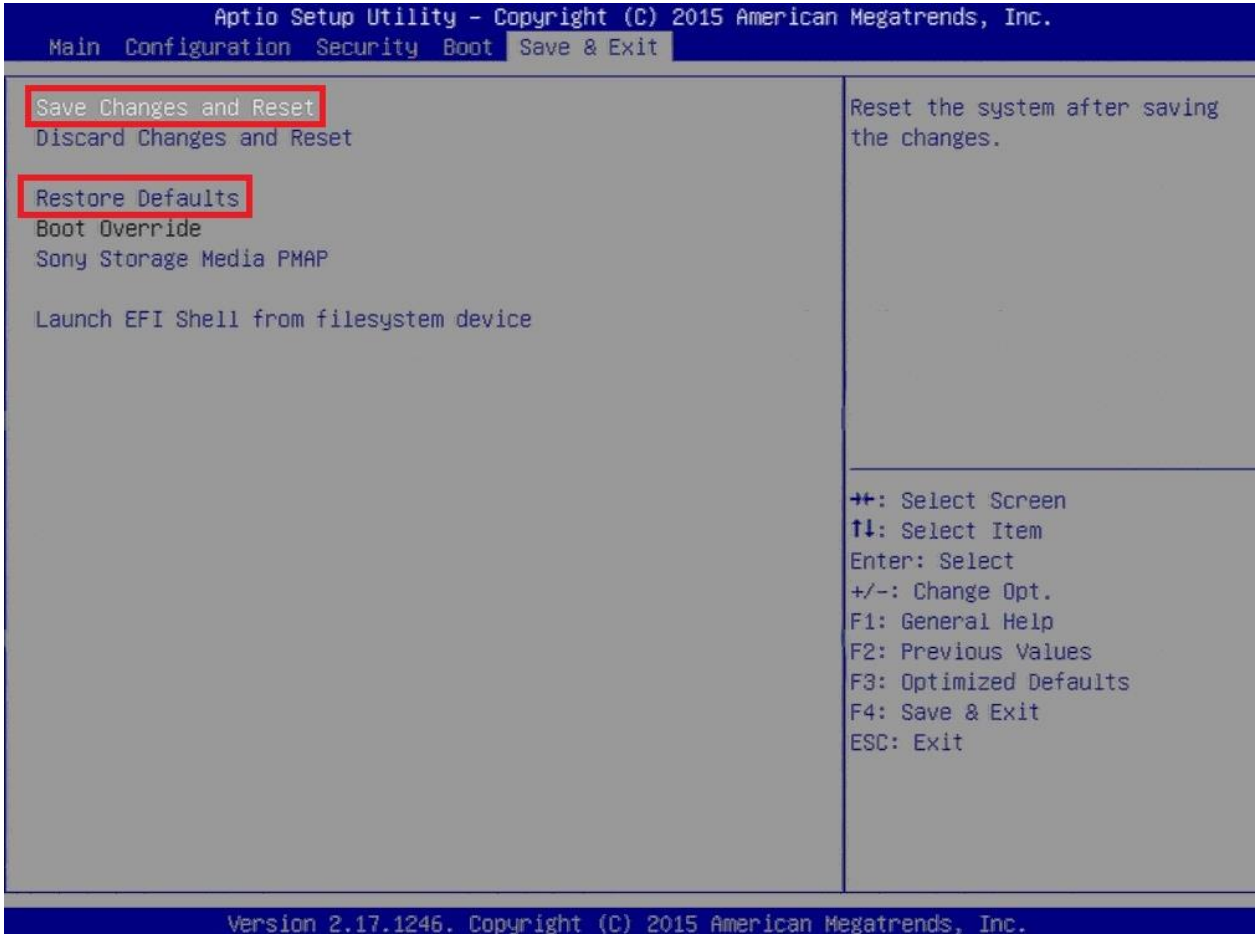
7. Update procedure



8. Complete the update



9. Power off the system (wait 10 sec) and power on again to initial the BIOS
10. Press **“del”** key into the BIOS setup menu and switch to **“Save & Exit”** page then select **“Restore Defaults”** option and press **“Yes”** then select **“Save Changes and Reset”** to finish all BIOS update processes.



Question: What are the display options while using NANO-6050?

Answer: The NANO-6050 does not support DVI display output .

It supports: 1. 1x dual channel 24bit LVDS on board connector via PTN3460 eDP to LVDS transmitter.

2. 2x mini DP connector from DP signal

Pin No.	Signal Description
1	+5V
2	BL_CTRL
3	+12V
4	Ground
5	BL Enable

PIN No.	Signal Description	PIN No.	Signal Description
1	VDD_LVDS	2	VDD_LVDS
3	LVDSA_DATA0	4	LVDSA_DATA#0
5	LVDSA_DATA1	6	LVDSA_DATA#1
7	LVDSA_DATA2	8	LVDSA_DATA#2
9	LVDSA_DATA3	10	LVDSA_DATA#3
11	LVDSA_CLKP	12	LVDSA_CLKN
13	DDC_SCL	14	DDC_SDA
15	GND	16	GND
17	LVDSB_DATA0	18	LVDSB_DATA#0
19	LVDSB_DATA1	20	LVDSB_DATA#1
21	LVDSB_DATA2	22	LVDSB_DATA#2
23	LVDSB_DATA3	24	LVDSB_DATA#3
25	LVDSB_CLKP	26	LVDSB_CLKN

Question: How to install Windows 7 in NANO-6050?

Answer: Windows 7* installation media does not include native driver support for USB 3.0, so during installation, when you get to the screen to select your preferred language, a keyboard or mouse connected to a USB 3.0 port does not respond. If you need the solution for this issue, please fill in the technical request form as below hyperlink and we will contact you as soon as possible.
http://www.portwell.com.tw/support/problem_report.php

Note:

Please visit our DownloadCenter to get the Catalog, User manual, BIOS, and driver files.
http://www.portwell.com.tw/support/download_center.php
If you have other additional technical information or request which is not covered in this manual, please fill in the technical request form as below hyperlink.
http://www.portwell.com.tw/support/problem_report.php
We will do our best to provide a suggestion or solution for you.
Thanks

9 Portwell Software Service

Portwell Evaluation Tool (PET)

The Portwell Evaluation Tool (PET) is an API which Portwell's customers can access the GPIO, I2C, SMBus, etc under Windows and Linux OS. For more information please contact Portwell.

Portwell BIOS web Tool (PBT)

The Portwell BIOS web Tool (PBT) is a brand new on-line utility which innovated by Portwell. PBT now is available for Portwell's premiere customers who are able to add customized BIOS logo andchange BIOS default settings on American Megatrends (AMI) BIOS.Please contact Portwell for more information.

Portwell EC Auto Test Tool (PECAT)

The Portwell EC Auto Test Tool (PECAT) is a brand new utility which innovated by Portwell. PECAT now is available for Portwell's premiere customers, who are able to Test Embedded Controller Function in UEFI Mode.Please contact Portwell for more information.

10 Industry Specifications

The list below provides links to industry specifications that apply to Portwell modules.

Low Pin Count Interface Specification, Revision 1.0 (LPC)http://www.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0http://www.usb.org/home
PCI Specification, Revision 2.3https://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0http://www.serialata.org/
PCI Express Base Specification, Revision 2.0https://www.pcisig.com/specifications